

A-NOTE 2.0 Block Diagram

PCB Layer Stackup

L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

VGA_CORE_S0 49
ISL6268

INPUT	OUTPUT
<i>DCBATOUT</i>	<i>VGA_CORE_S0</i>

Battery Charger

<i>INPUTS</i>	<i>OUTPUTS</i>
<i>AD+</i> <i>BAT+</i>	<i>DCBATOUT</i>

SYSTEM DC/DC
TPS 51120

INPUT	OUTPUT
<i>DCBATOUT</i>	<i>5V_S5</i> <i>3D3V_S5</i>

SYSTEM DC/DC
APL5332KAC

INPUT	OUTPUT
3D3V_S5	1D2V_S5

SYSTEM POWER
TPS51116

INPUT	OUTPUT
DCBATOUT	1D8V_S3 0D9V_S3

1D2V S0

INPUT	OUTPUT
DCBATOUT	1D2V_S0

CPU V CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S

SYSTEM POWER
TPS 51120

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BLOCK DIAGRAM

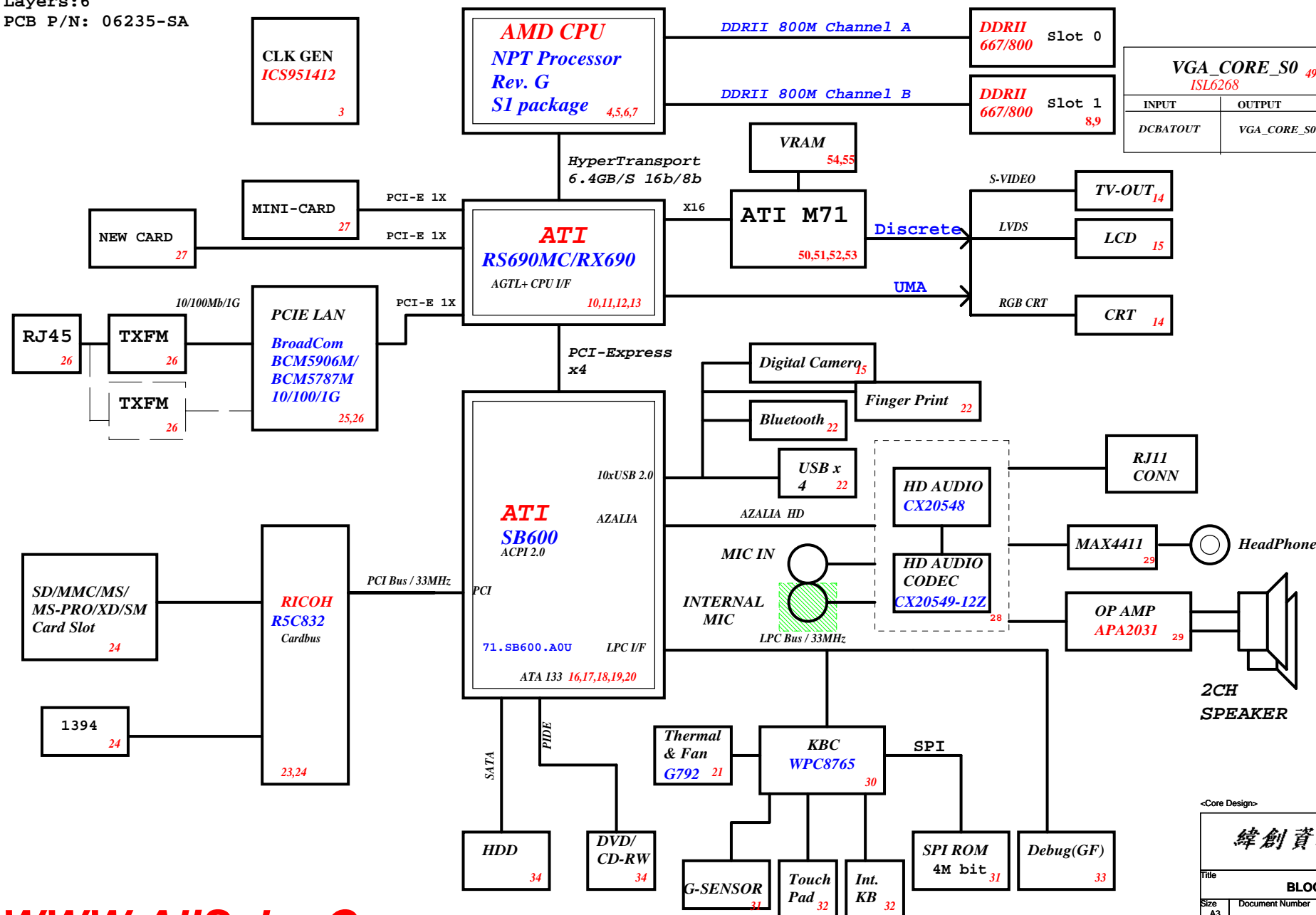
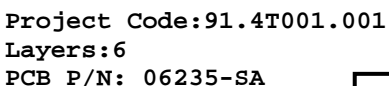
Size
A2

Document Number

A-NOTE2.0-AMD

Date: Tuesday, September 26, 2006

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SA: 07/31/06 Start

<Core Design>

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Title

CHANGE HISTORY

Size
A3

Document Number
A-NOTE2.0-AMD

Rev
SA

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<Core Design>

緯創資通 Wistron Corporation
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Title		CPU(1/4)_HyperTransport I/F	
Size	Document Number	Rev	
A3	A-NOTE2.0-AMD	SA	
Date:	Tuesday, September 26, 2006	Sheet	4 of 55

8 M_A_DQ[63.0]

8 M_B_DQ[63.0]

U66C

U66B

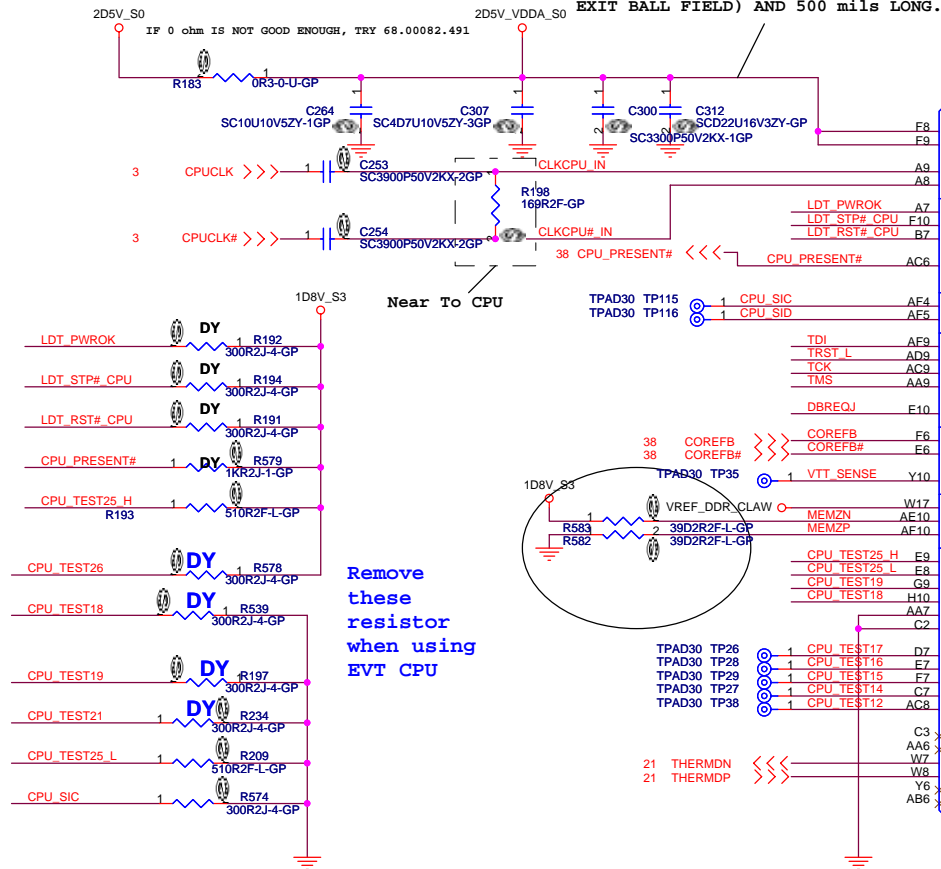
MEMORY
INTERFACE

MEMORY
INTERFACE

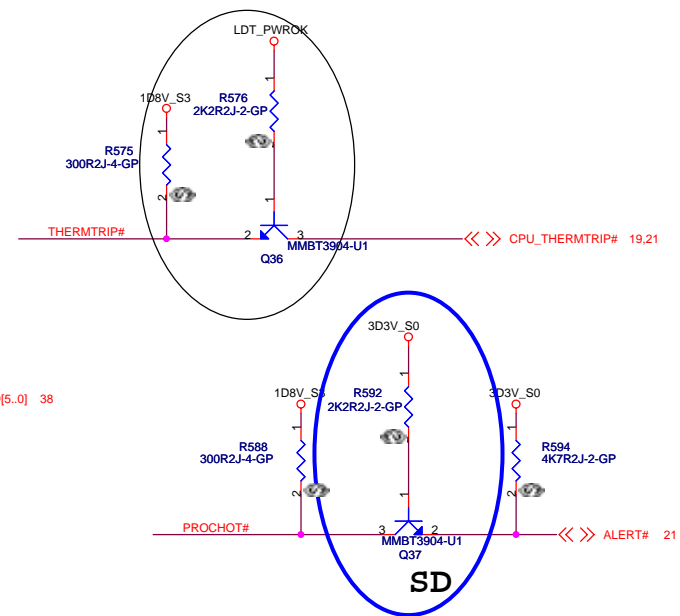
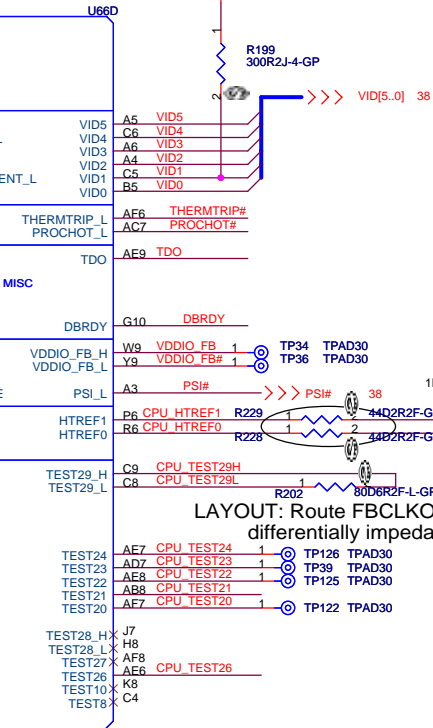
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Taipei Hsien 221, Taiwan, R.O.C.

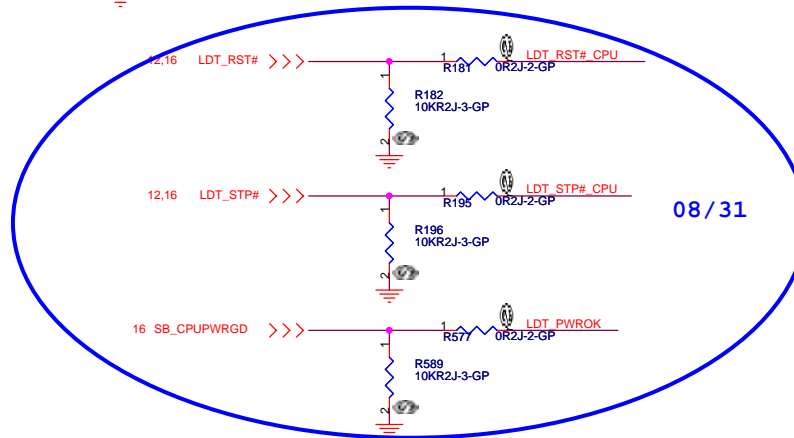
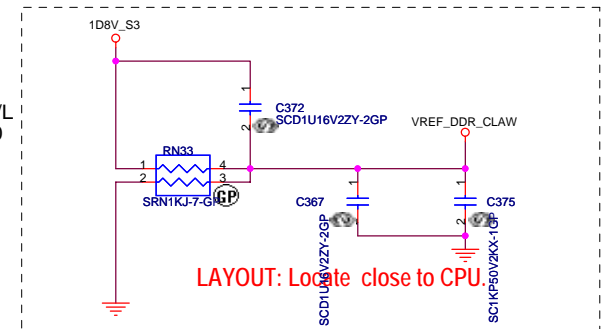
Title			
CPU(2/4)_DDR			
Size	Document Number		Rev
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ROUTE VDDA TRACE APPROX.
WIDE(USE 2X25 mil TRACES TO
BALL FIELD) AND 500 mils LONG.



VREF_DDR_CLAW



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*Put decap near power(0.9V)
and pull-up resistor*



CLAW HAMMER TO NB

NB TO CLAW HAMMER

4 CPUCADOUT[15..0] >>>>
4 CPUCADOUTJ[15..0] >>>>

U65A 1 of 5

>>>> NB0CADOUT[15..0] 4
>>>> NB0CADOUTJ[15..0] 4

CPUCADOUT15	R19	HT_RXCAD15P
CPUCADOUT14	R18	HT_RXCAD15N
CPUCADOUT13	R21	HT_RXCAD14P
CPUCADOUT12	R22	HT_RXCAD14N
CPUCADOUT11	U22	HT_RXCAD13P
CPUCADOUT10	U21	HT_RXCAD13N
CPUCADOUT9	U18	HT_RXCAD12P
CPUCADOUT8	U19	HT_RXCAD12N
CPUCADOUT7	W19	HT_RXCAD11P
CPUCADOUT6	W20	HT_RXCAD11N
CPUCADOUT5	AC21	HT_RXCAD10P
CPUCADOUT4	AB22	HT_RXCAD10N
CPUCADOUT3	AB20	HT_RXCAD9P
CPUCADOUT2	AA20	HT_RXCAD8N
CPUCADOUT1	AA19	HT_RXCAD8P
CPUCADOUT0	Y19	HT_RXCAD8N
CPUCADOUT15	T24	HT_RXCAD7P
CPUCADOUT14	R25	HT_RXCAD7N
CPUCADOUT13	U25	HT_RXCAD6P
CPUCADOUT12	U24	HT_RXCAD6N
CPUCADOUT11	Y23	HT_RXCAD5P
CPUCADOUT10	U23	HT_RXCAD5N
CPUCADOUT9	Y24	HT_RXCAD4P
CPUCADOUT8	Y25	HT_RXCAD4N
CPUCADOUT7	AA25	HT_RXCAD3P
CPUCADOUT6	AA24	HT_RXCAD3N
CPUCADOUT5	AB23	HT_RXCAD2P
CPUCADOUT4	AA23	HT_RXCAD2N
CPUCADOUT3	AB24	HT_RXCAD1P
CPUCADOUT2	AB25	HT_RXCAD1N
CPUCADOUT1	AC24	HT_RXCAD0P
CPUCADOUT0	AC25	HT_RXCAD0N

HYPER TRANSPORT CPU
I/F

HT_TXCAD15P	P21	NB0CADOUT15
HT_TXCAD15N	P22	NB0CADOUT14
HT_TXCAD14P	P18	NB0CADOUT13
HT_TXCAD14N	P19	NB0CADOUT12
HT_TXCAD13P	M22	NB0CADOUT11
HT_TXCAD13N	M21	NB0CADOUT10
HT_TXCAD12P	M18	NB0CADOUT9
HT_TXCAD12N	M19	NB0CADOUT8
HT_TXCAD11P	L18	NB0CADOUT7
HT_TXCAD11N	L19	NB0CADOUT6
HT_TXCAD10P	G22	NB0CADOUT5
HT_TXCAD10N	G21	NB0CADOUT4
HT_TXCAD9P	J20	NB0CADOUT3
HT_TXCAD8N	J21	NB0CADOUT2
HT_TXCAD8P	F21	NB0CADOUT1
HT_TXCAD8N	F22	NB0CADOUT0

HT_TXCAD7P	N24	NB0CADOUT15
HT_TXCAD7N	N25	NB0CADOUT14
HT_TXCAD6P	L25	NB0CADOUT13
HT_TXCAD6N	M24	NB0CADOUT12
HT_TXCAD5P	K25	NB0CADOUT11
HT_TXCAD5N	K24	NB0CADOUT10
HT_TXCAD4P	K23	NB0CADOUT9
HT_TXCAD4N	G25	NB0CADOUT8
HT_TXCAD3P	H24	NB0CADOUT7
HT_TXCAD3N	F25	NB0CADOUT6
HT_TXCAD2P	F24	NB0CADOUT5
HT_TXCAD2N	E24	NB0CADOUT4
HT_TXCAD1P	E23	NB0CADOUT3
HT_TXCAD1N	F23	NB0CADOUT2
HT_TXCAD0P	E24	NB0CADOUT1
HT_TXCAD0N	E25	NB0CADOUT0

4 CPUHTTCLKOUT1 >>>>
4 CPUHTTCLKOUTJ1 >>>>

4 CPUHTTCLKOUT0 >>>>
4 CPUHTTCLKOUTJ0 >>>>

4 CPUHTTCTLOUT0 >>>>
4 CPUHTTCTLOUTJ0 >>>>

4 CPUHTTCTLOUT0 >>>>
4 CPUHTTCTLOUTJ0 >>>>

4 NB0HTTCLKOUT1 >>>>
4 NB0HTTCLKOUTJ1 >>>>

4 NB0HTTCLKOUT0 >>>>
4 NB0HTTCLKOUTJ0 >>>>

4 NB0HTTCTLOUT >>>>
4 NB0HTTCTLOUTJ >>>>

VDDHT_PKG

R550 1
R208 1

49D9R2F-GP HT_RXCALP A24
49D9R2F-GP HT_RXCALN C24

HT_RXCLK1P W21
HT_RXCLK1N W22
HT_RXCLK0P Y24
HT_RXCLK0N W25
HT_RXCTL P24
HT_RXCTLN P25
HT_RXCALP A24
HT_RXCALN C24

RS690M-GP

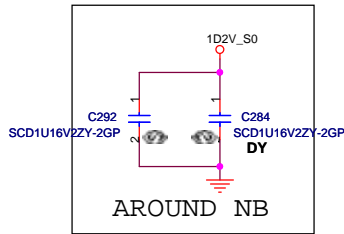
71.RS690.M01

HT_TXCLK1P I21
HT_TXCLK1N L22
HT_TXCLK0P J24
HT_TXCLK0N J25
HT_TXCTL N23
HT_TXCTLN P23
HT_TXCALP C25
HT_TXCALN D24

HT_TXCLK1P I21
HT_TXCLK1N L22
HT_TXCLK0P J24
HT_TXCLK0N J25
HT_TXCTL N23
HT_TXCTLN P23
HT_TXCALP C25
HT_TXCALN D24

HT_TXCLK1P I21
HT_TXCLK1N L22
HT_TXCLK0P J24
HT_TXCLK0N J25
HT_TXCTL N23
HT_TXCTLN P23
HT_TXCALP C25
HT_TXCALN D24

Close to NB ball



Close to NB ball

<Core Design>

緯創資通

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Title

NB-RS690M HT

Size

A3 Document Number

A-NOTE2.0-AMD

Rev

SA

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50 PCIE_GFX_RXN[15..0] >>

50 PCIE_GFX_RXP[15..0] >>

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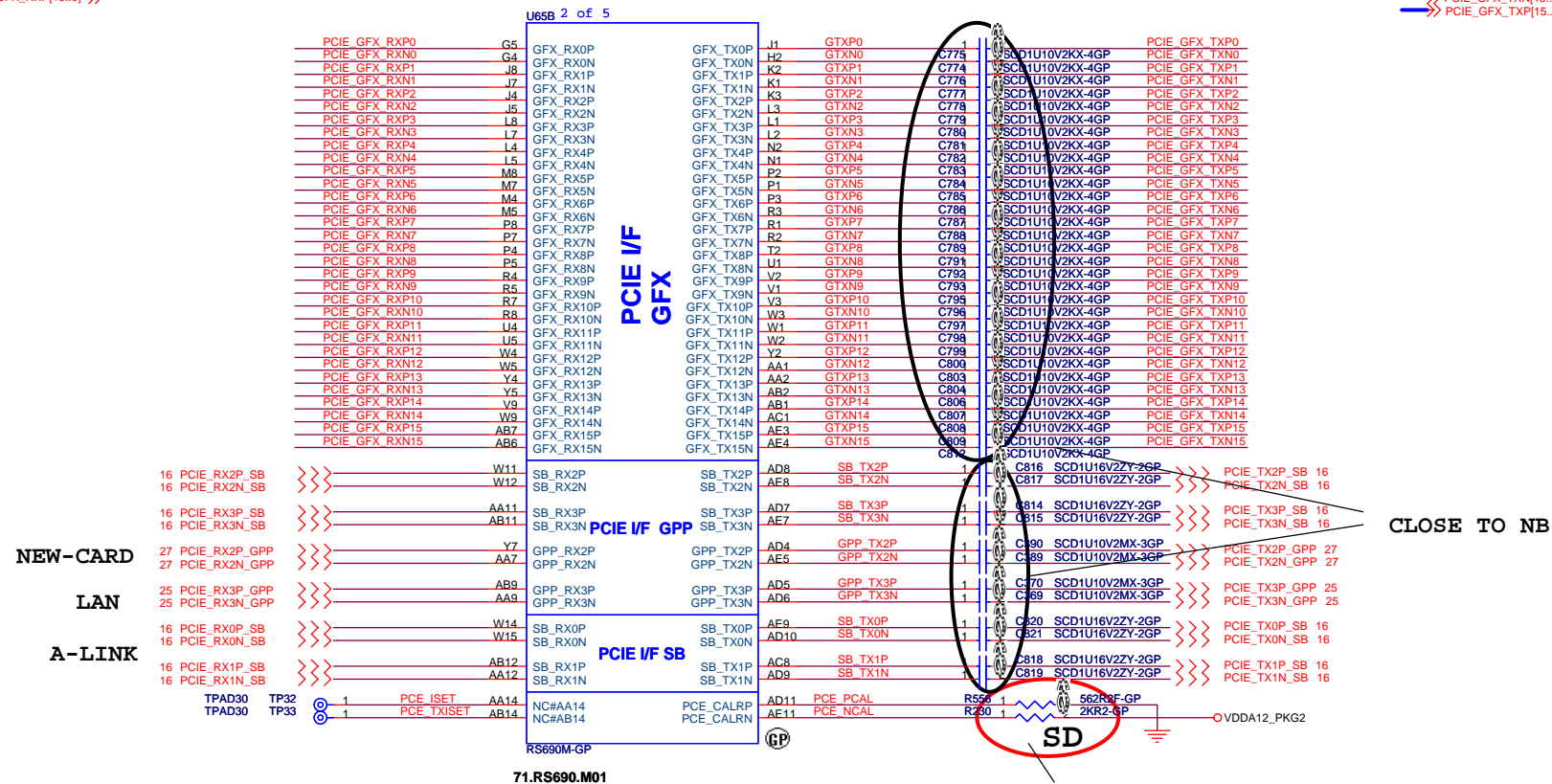
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==> PCIE_GFX_TXP[15..0] 50

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--> PCIE_GFX_TXN[15..0] 50
--> PCIE_GFX_TXP[15..0] 50

```



Close to NB ball

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

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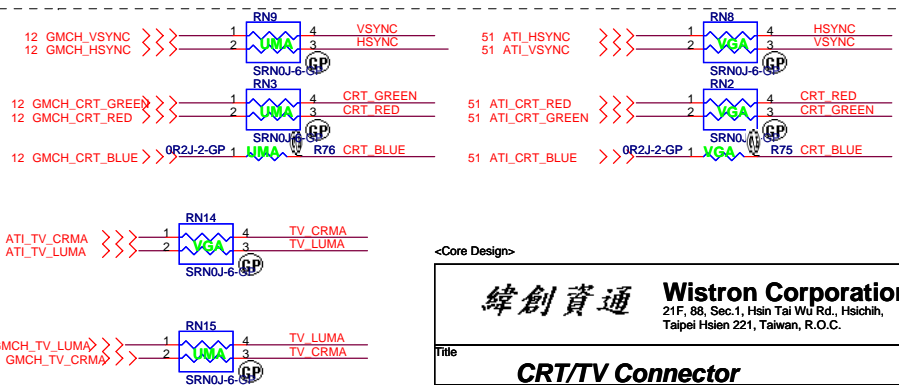
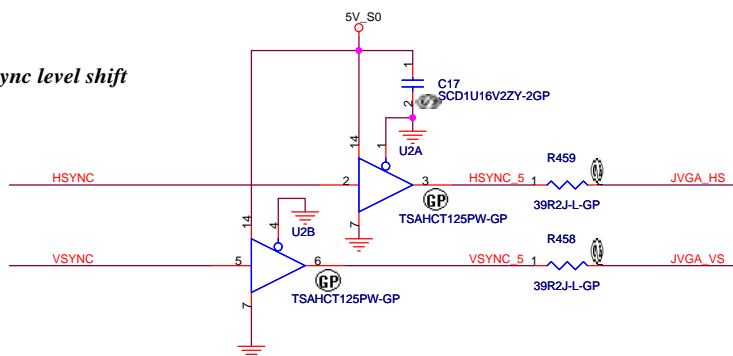
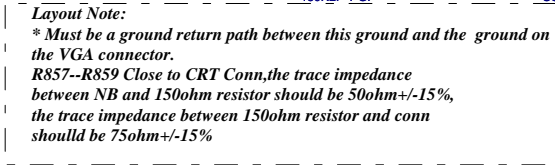
Title	NB-RS690M MEM/PCIE LINK I/F
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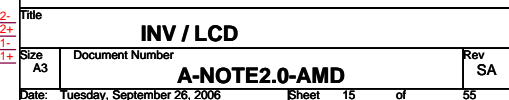


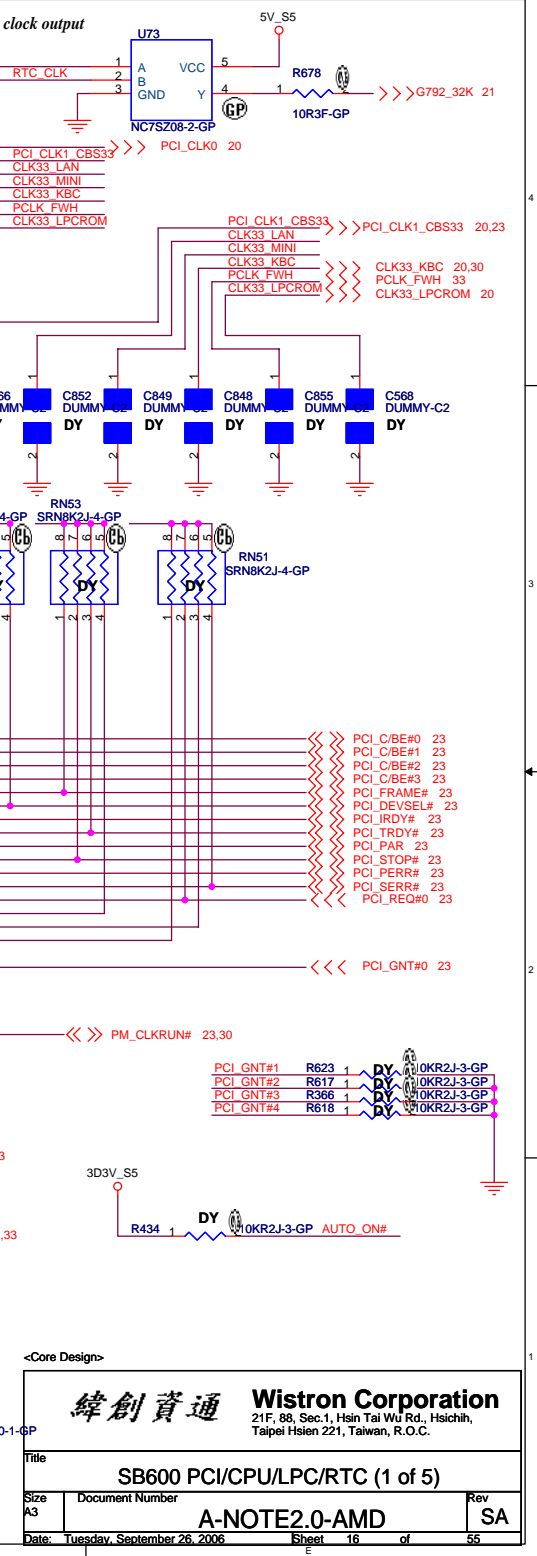
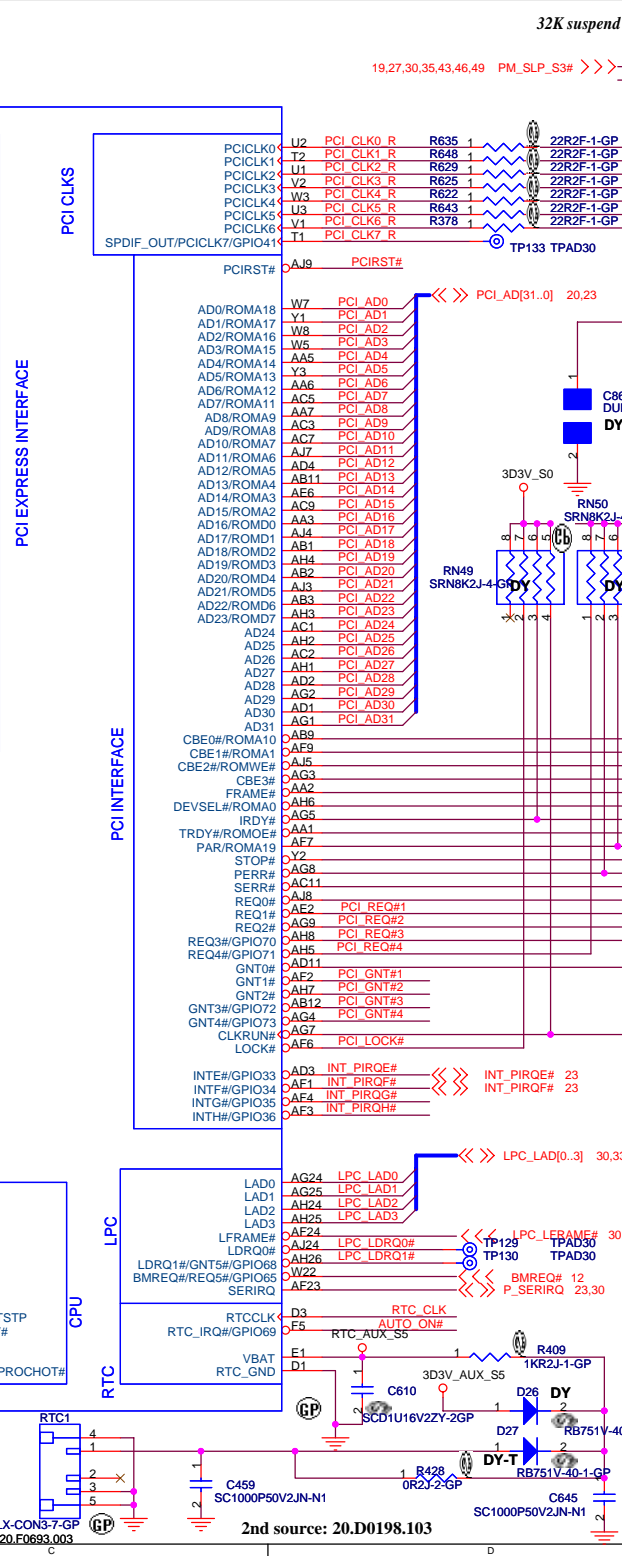
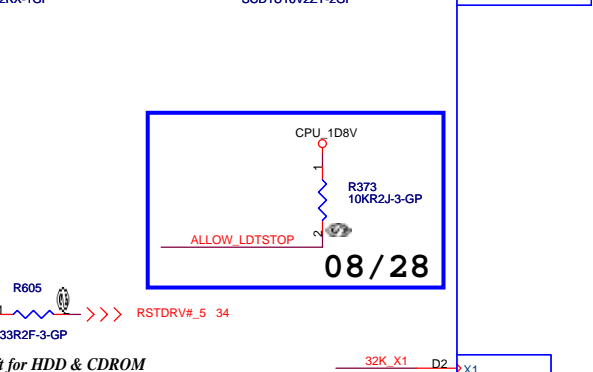
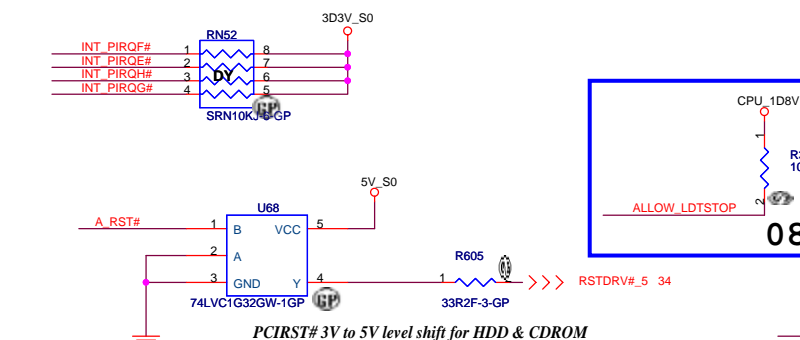
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CRT/TV Connector				
Size A3	Document Number			Rev
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TOP VIEW

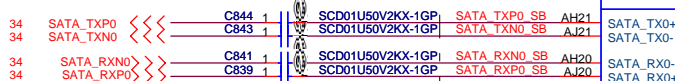
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LCD

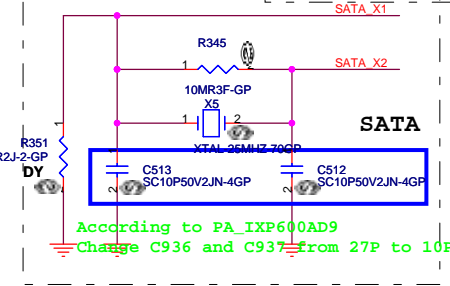




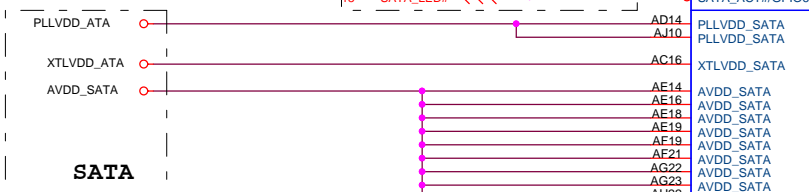
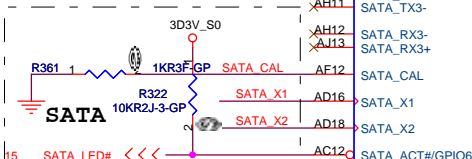
PLACE SATA AC DECOUPLING CAPS CLOSE TO SB460



SATA

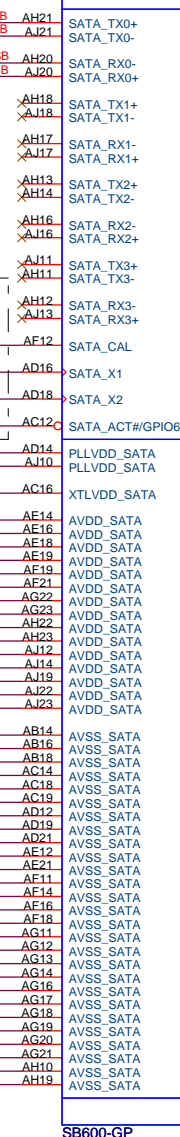


According to PA_IXP600AD9
Change C936 and C937 from 27P to 10P.



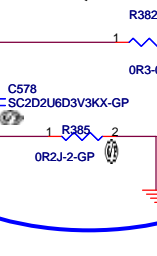
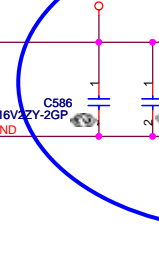
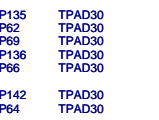
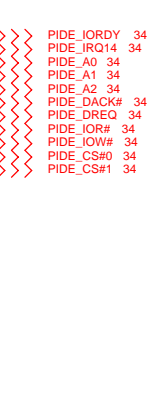
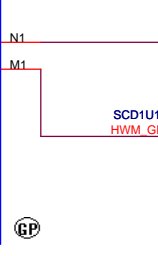
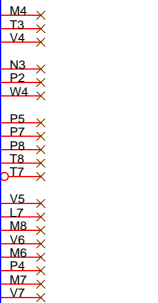
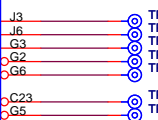
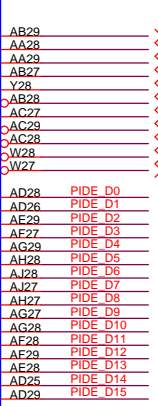
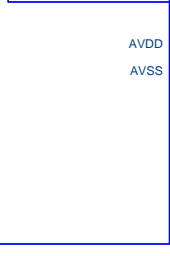
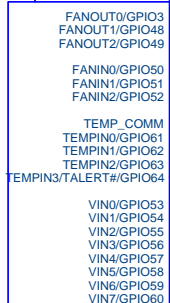
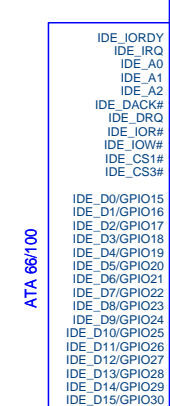
SATA

U71B 2 of 4

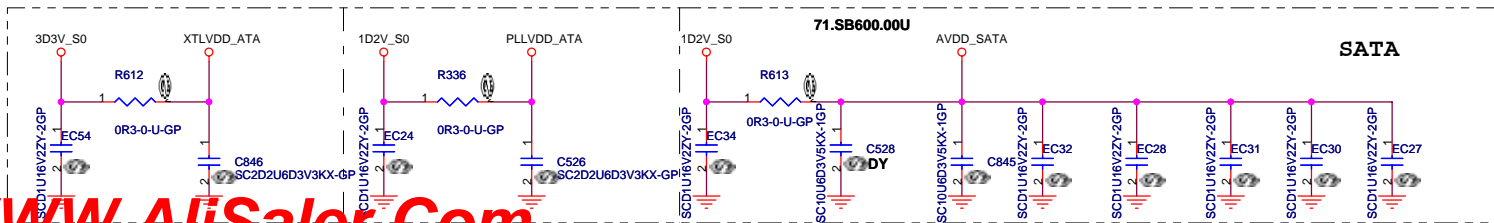
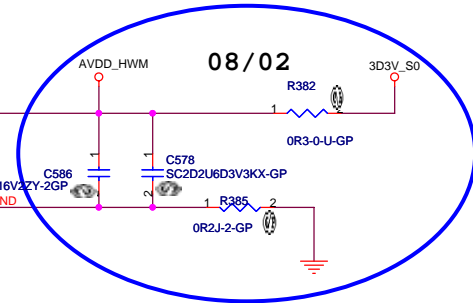


SERIAL ATA

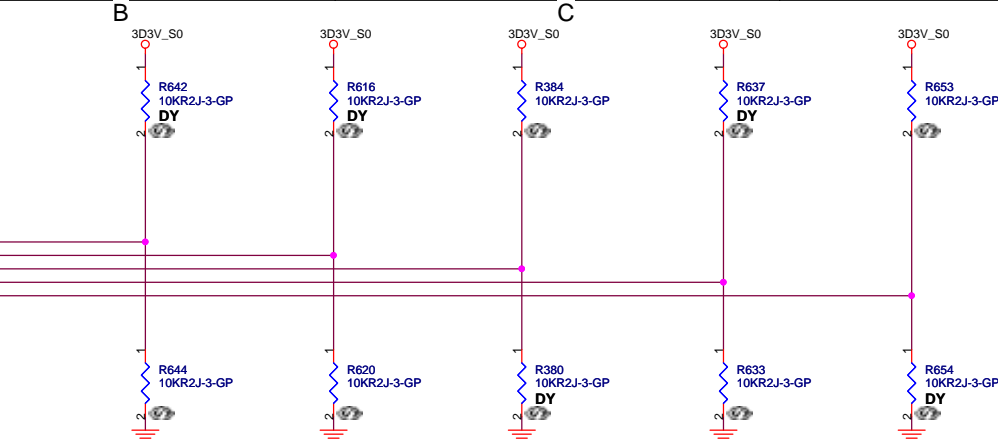
SERIAL ATA POWER



PIDE_D[15..0] 34



19,28 ACZ_SDOUT
16,30 CLK33_KBC
16 CLK33_LPCROM
16 PCI_CLK0
16,23 PCI_CLK1_CBS33

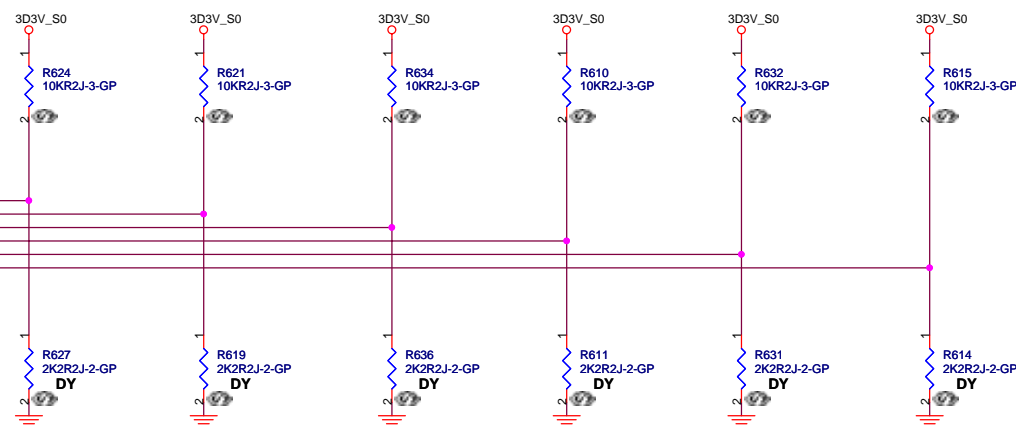


REQUIRED SYSTEM STRAPS

		AC_SDOUT	PCI_CLK0,PCI_CLK1_CBS33	PCI_CLK4	PCI_CLK6
STRAP HIGH		USE DEBUG STRAPS	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I	USB INT PLL48	CPU I/F=K8 DEFAULT
STRAP LOW		IGNORE DEBUG STRAPS DEFAULT	L,H=LPC ROM II L,L=Firmware Hub ROM	USB EXT. 48MHZ DEFAULT	CPU I/F=P4

SB600 HAS 15K INTERNAL PU FOR PCI_AD[23..28]

16,23 PCI_AD28
16,23 PCI_AD27
16,23 PCI_AD26
16,23 PCI_AD25
16,23 PCI_AD24
16,23 PCI_AD23



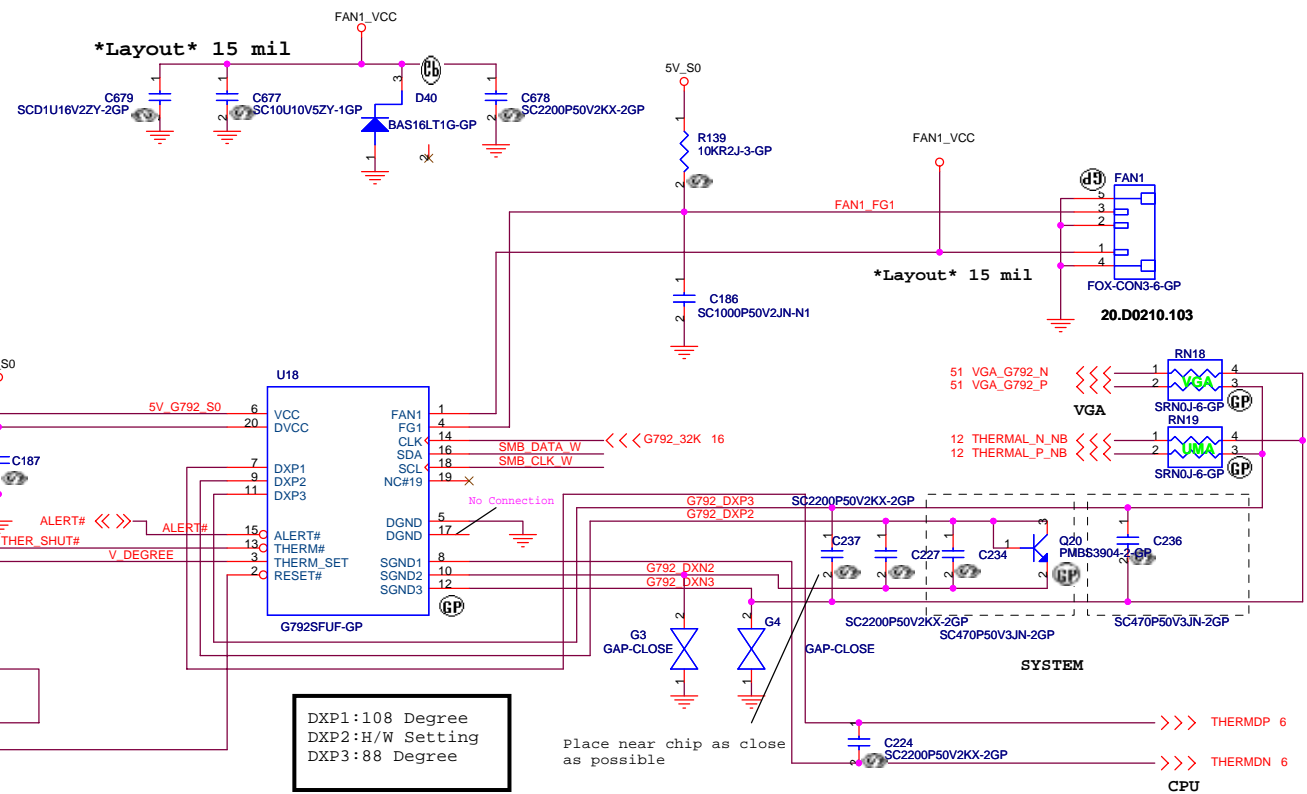
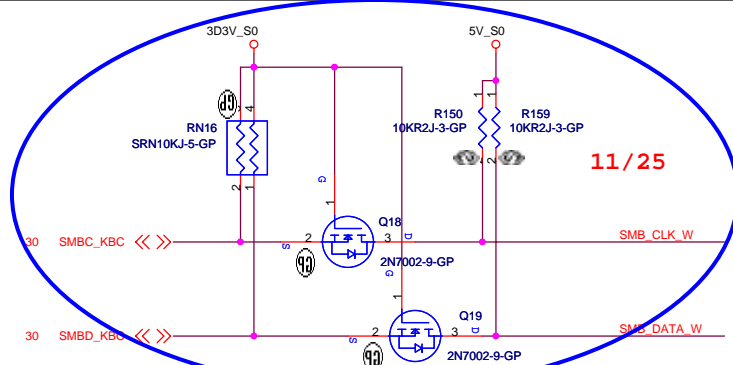
DEBUG STRAPS

		PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH		RESERVED	RESERVED	RESERVED	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOT FAIL TIMER DISABLE DEFAULT
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOT FAIL TIMER ENABLE

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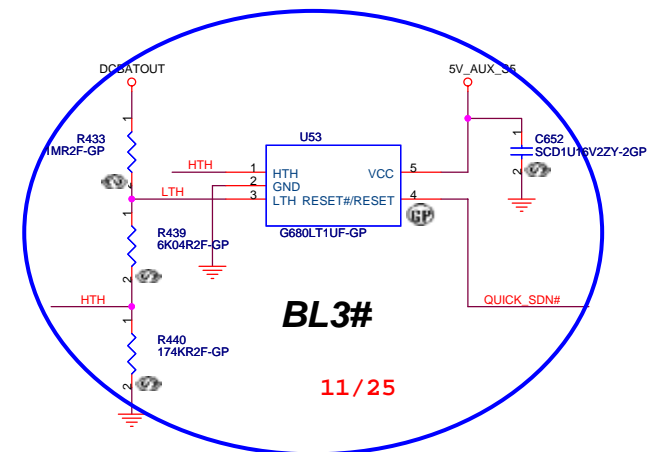
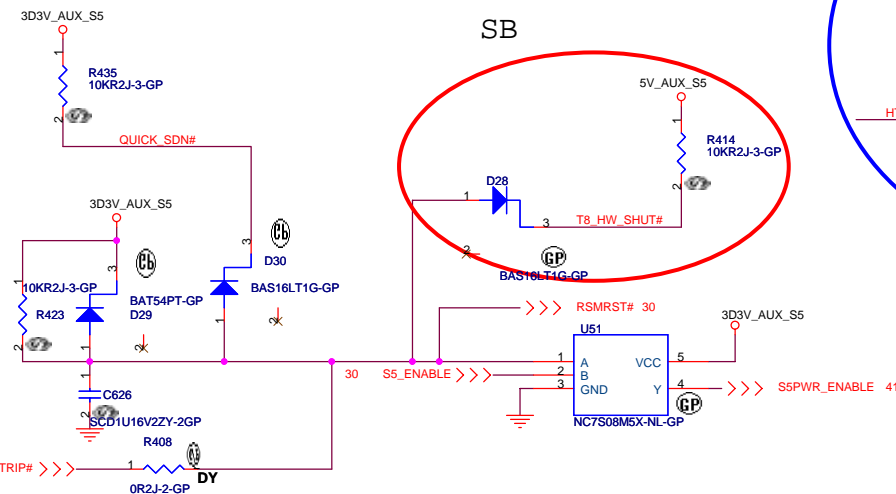
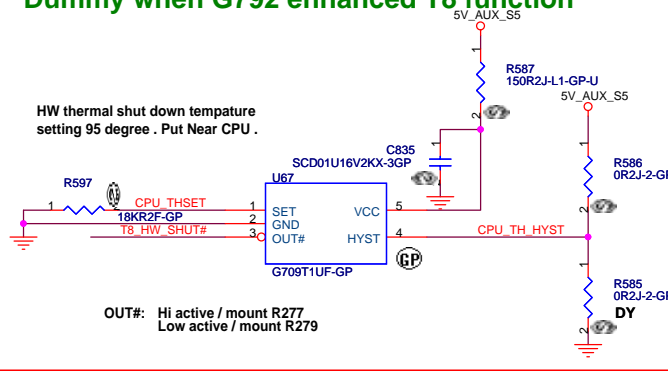
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Size A3	Document Number	A-NOTE2.0-AMD	
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HW Thermal Throttling

Dummy when G792 enhanced T8 function

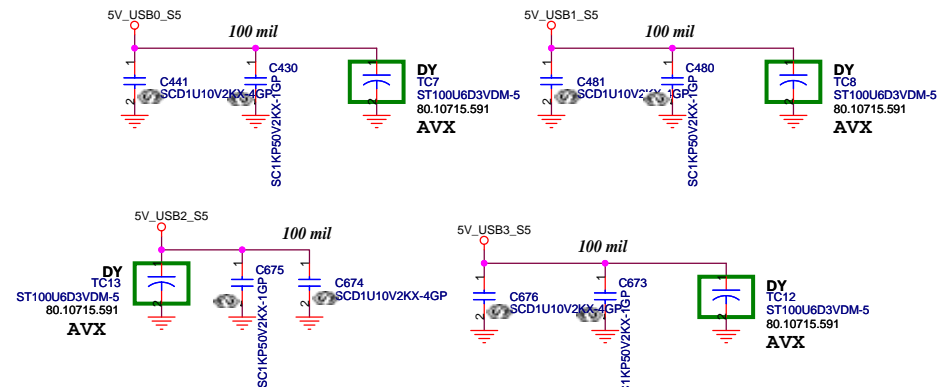
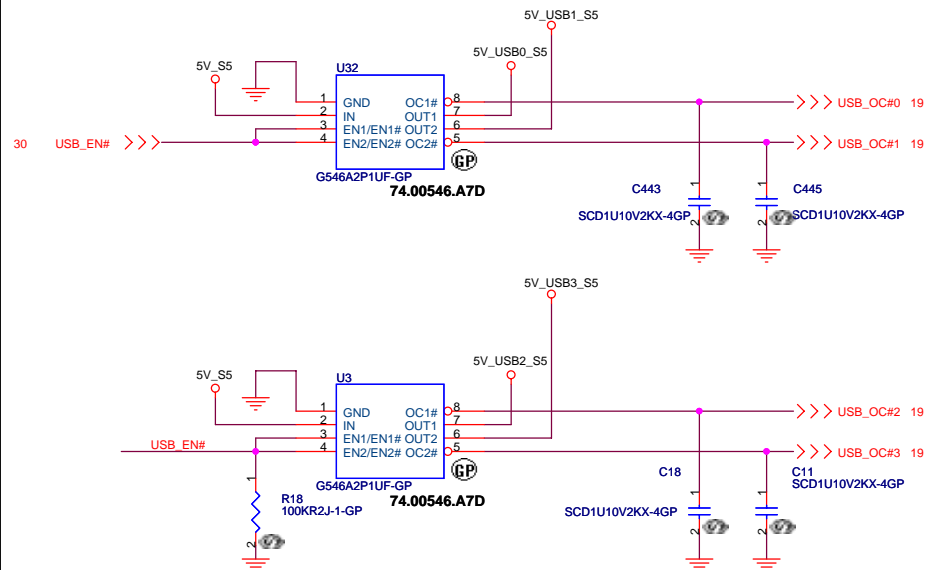
HW thermal shut down temperature setting 95 degree . Put Near CPU .



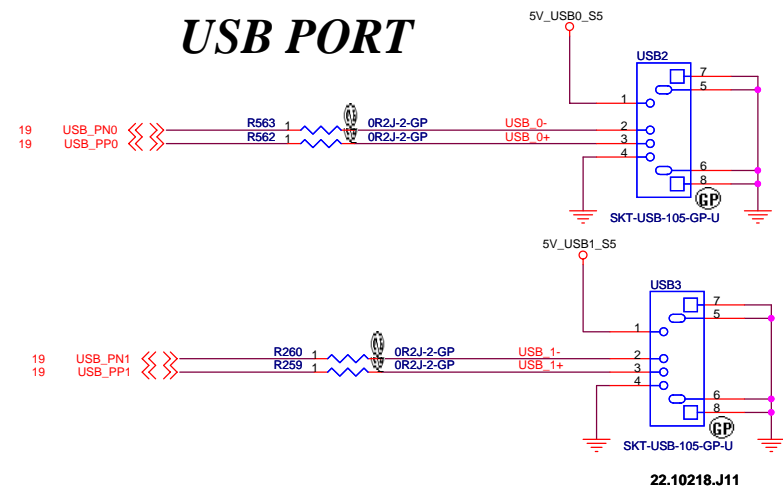
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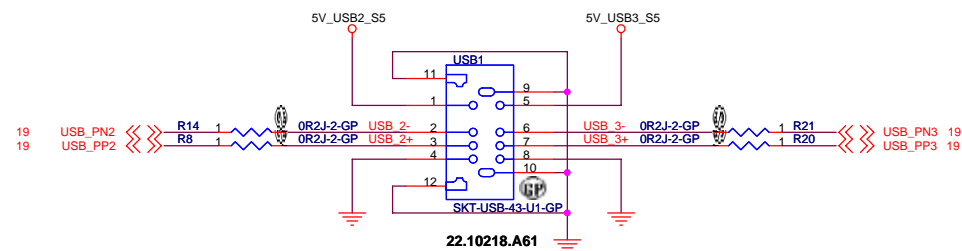
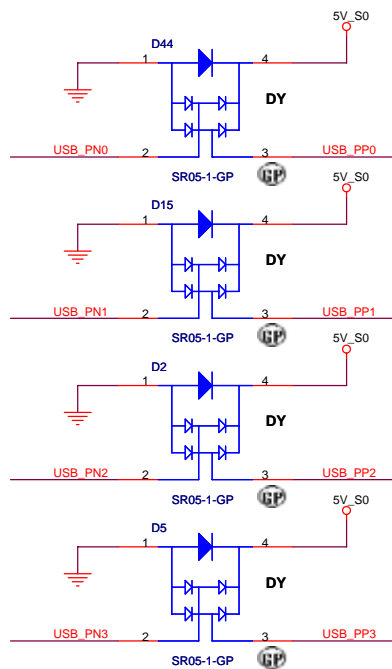
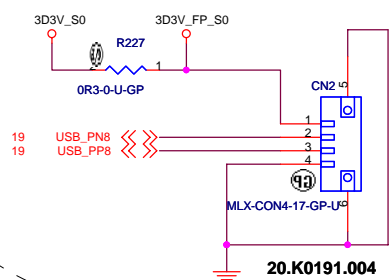
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A3	A-NOTE2.0-AMD	SA	
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USB PORT



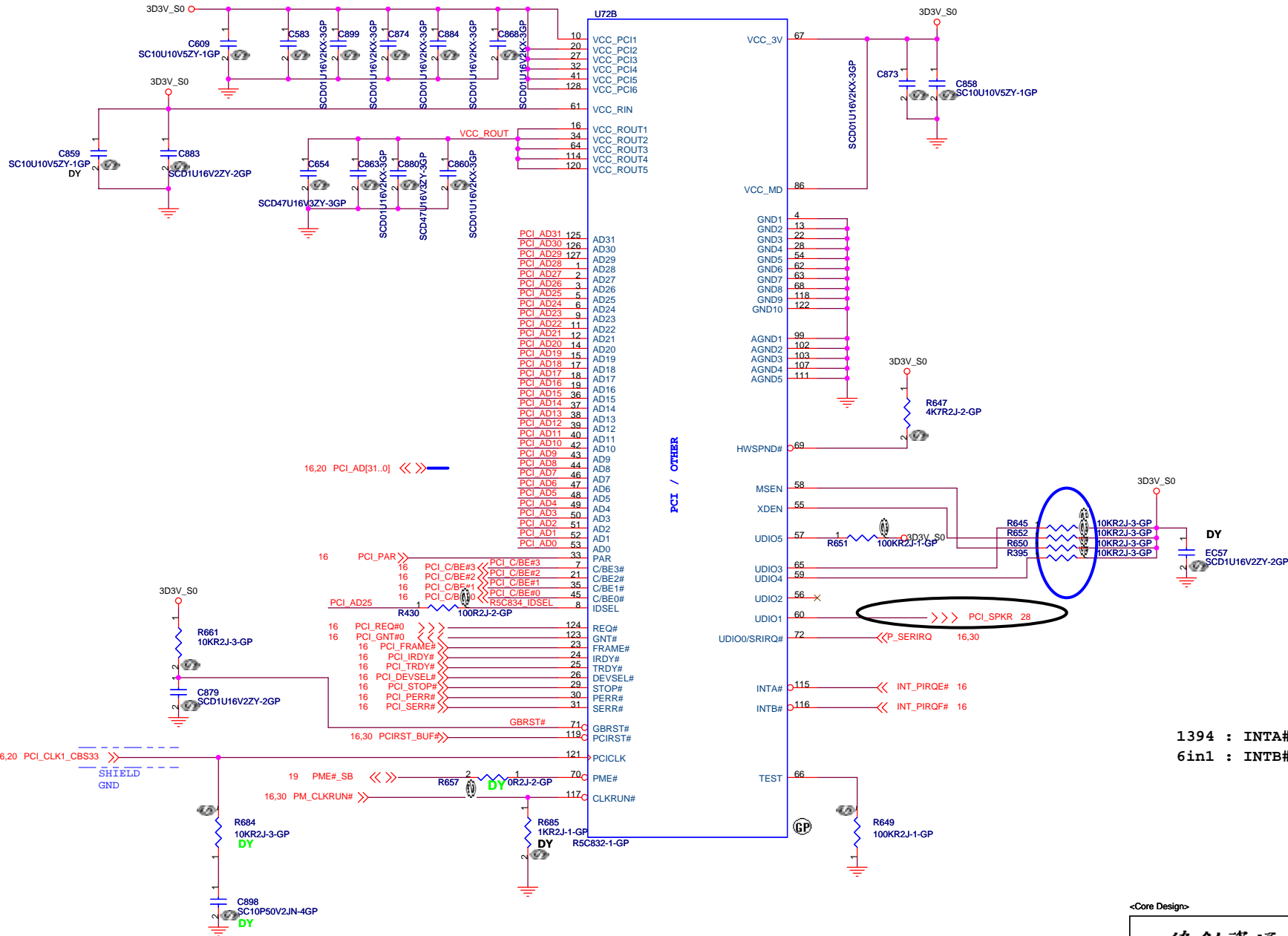
Finger Printer CNN



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB/MDC/BT and TV TURNER I/F		
Size	Document Number	Rev
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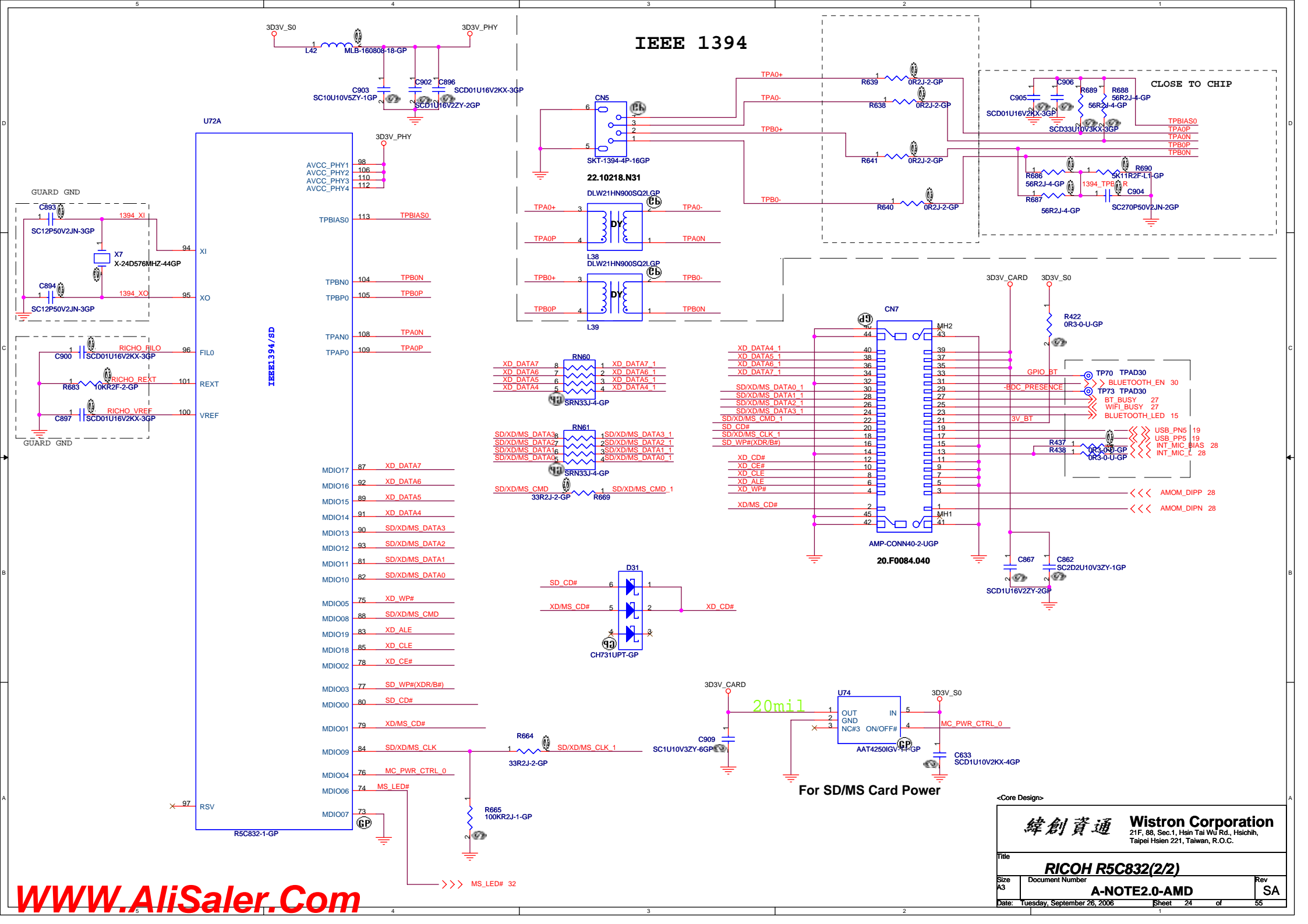


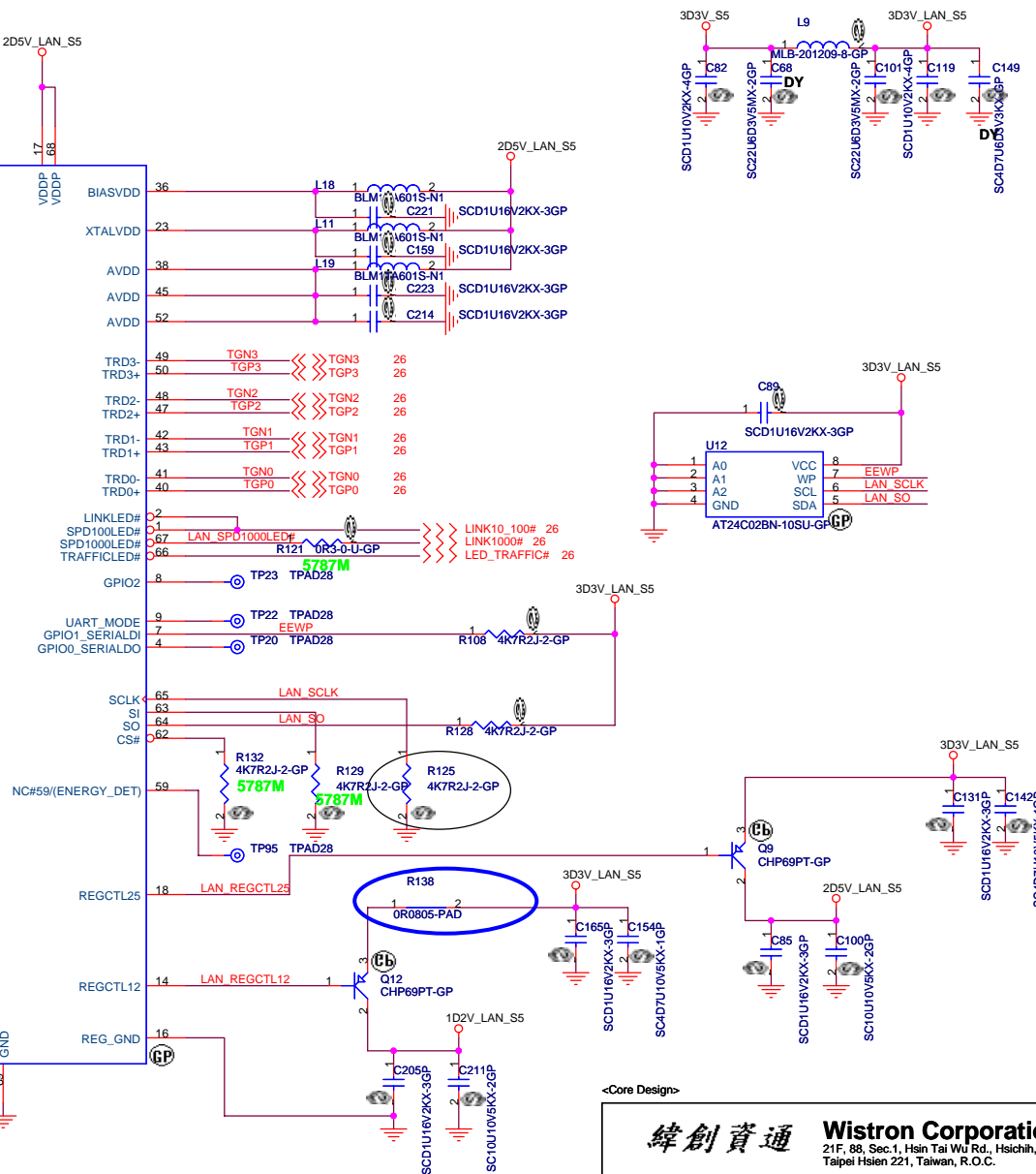
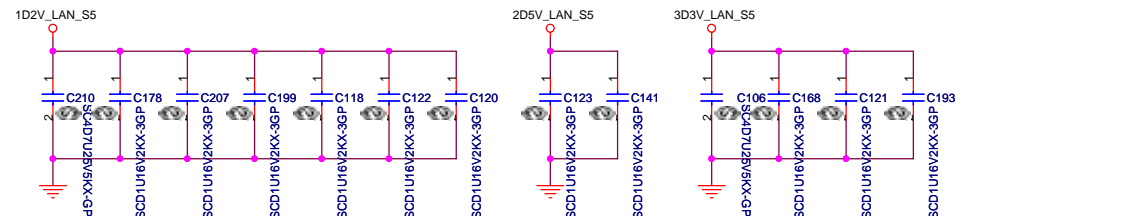
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Taipei Hsien 221, Taiwan, R.O.C.

Title		RICOH R5C832(1/2)	
Size	Document Number	A-NOTE2.0-AMD	
A3		SA	
Date:	Tuesday, September 26, 2006	Sheet	23 of 55

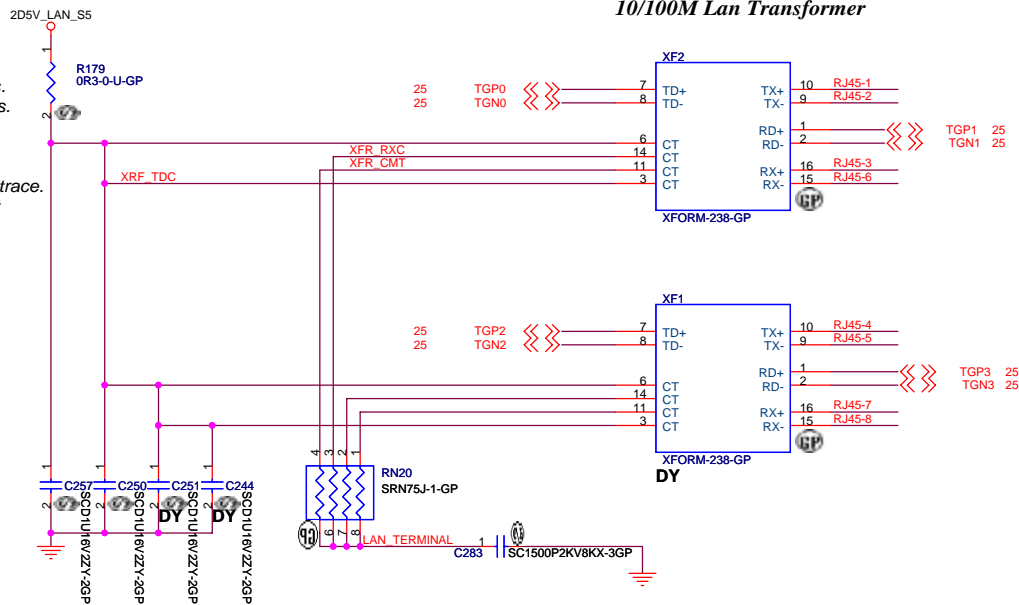
IEEE 1394



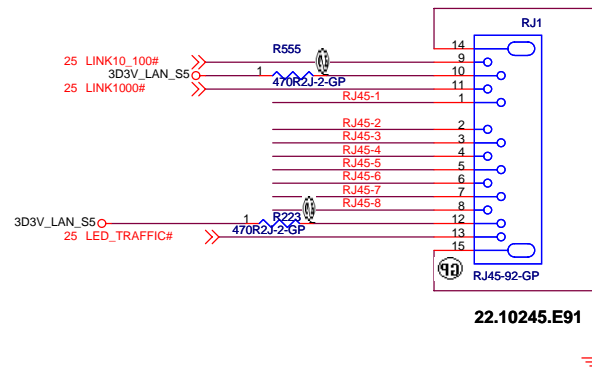
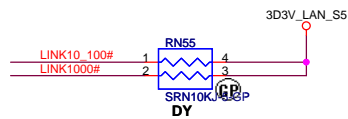


WWW.AliSaler.Com

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



PIN09 : GREEN
PIN11 : ORANGE

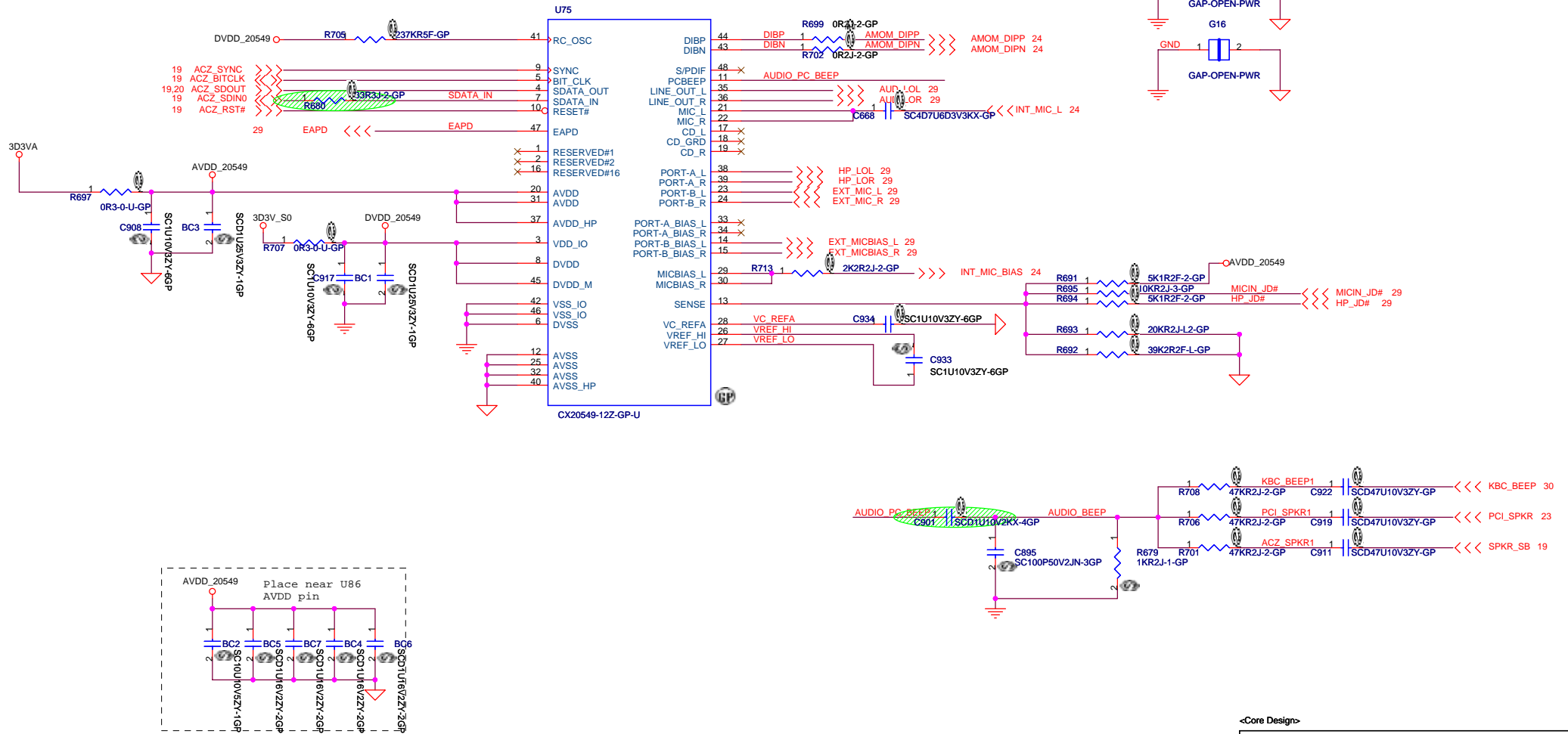


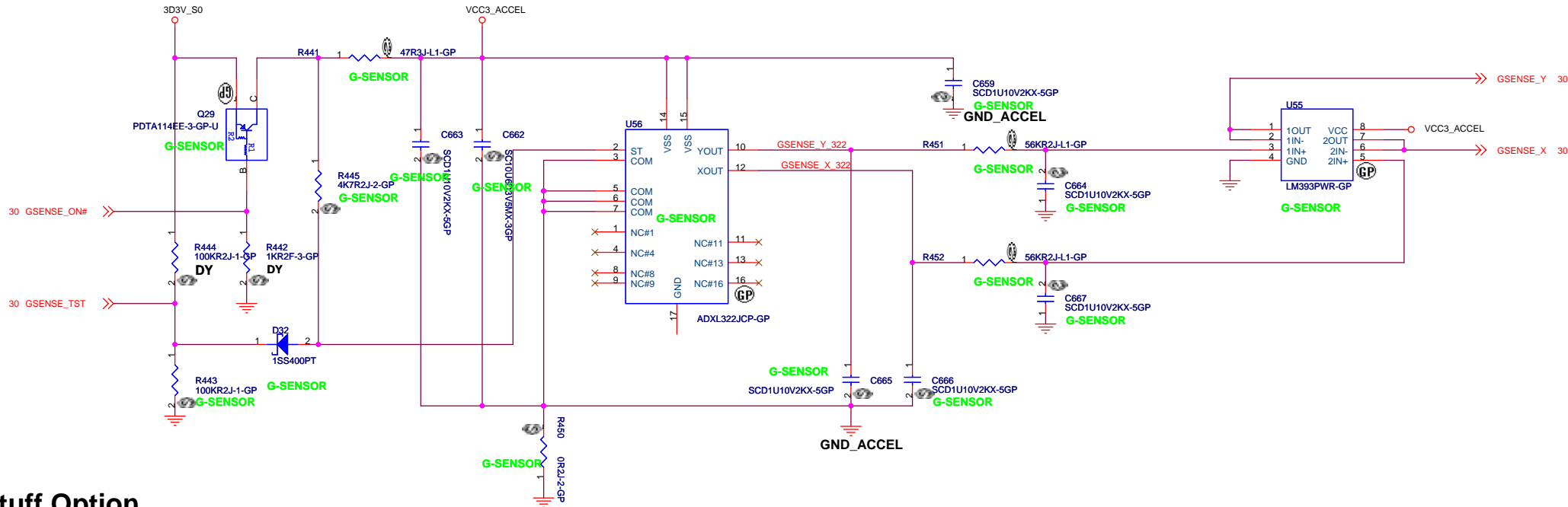
Green : Link up
Blinking : TX/RX activity

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		LAN Connector	
Size	Document Number	A-NOTE2.0-AMD	
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Date:	Tuesday, September 26, 2006	Sheet	26 of 55



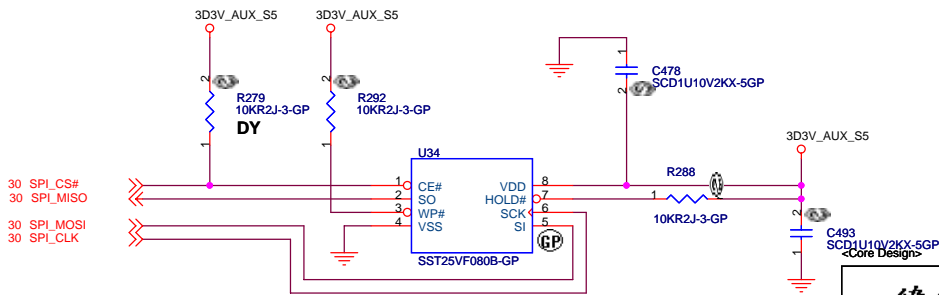


Stuff Option

RP-1	ADXL322	STMicro	No Accel.
R172	ASM	ASM	NO_ASM
R173	ASM	ASM	NO_ASM
U9	NO_ASM	LIS2L02AL	NO_ASM
Q105	ASM	ASM	NO_ASM
D97	ASM	ASM	NO_ASM
R956	NO_ASM	ASM	NO_ASM
R62	ASM	ASM	NO_ASM
R885	10 Ohm	10 Ohm	NO_ASM
C829	ASM	ASM	NO_ASM
C969	ASM	ASM	NO_ASM
R959	ASM	ASM	NO_ASM
C830	NO_ASM	0.033UF	NO_ASM
C847	NO_ASM	0.033UF	NO_ASM

RP-1	ADXL322	STMicro	No Accel.
R969	56K	56K	NO_ASM
C938	ASM	ASM	NO_ASM
R970	56K	56K	NO_ASM
C956	ASM	ASM	NO_ASM
U66	ADXL322	NO_ASM	NO_ASM
C170	ASM	NO_ASM	NO_ASM
C178	ASM	NO_ASM	NO_ASM
C190	ASM	NO_ASM	NO_ASM
R31	ASM	NO_ASM	NO_ASM

SPI ROM for System & KBC

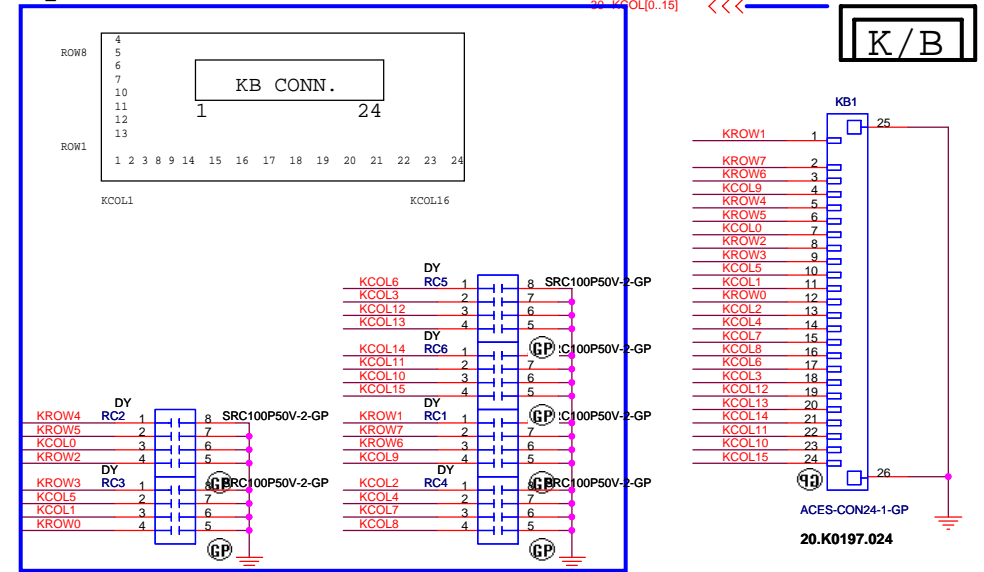
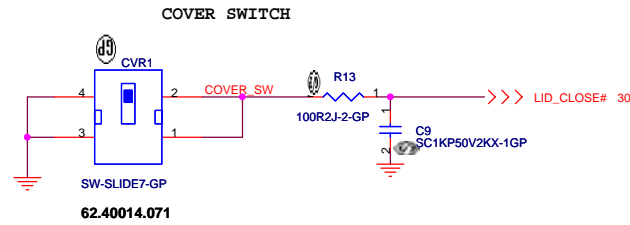


1. SST 25VF016B
2. Macronix MX25L1605A
3. SST 8Mbit 72.25080.G01

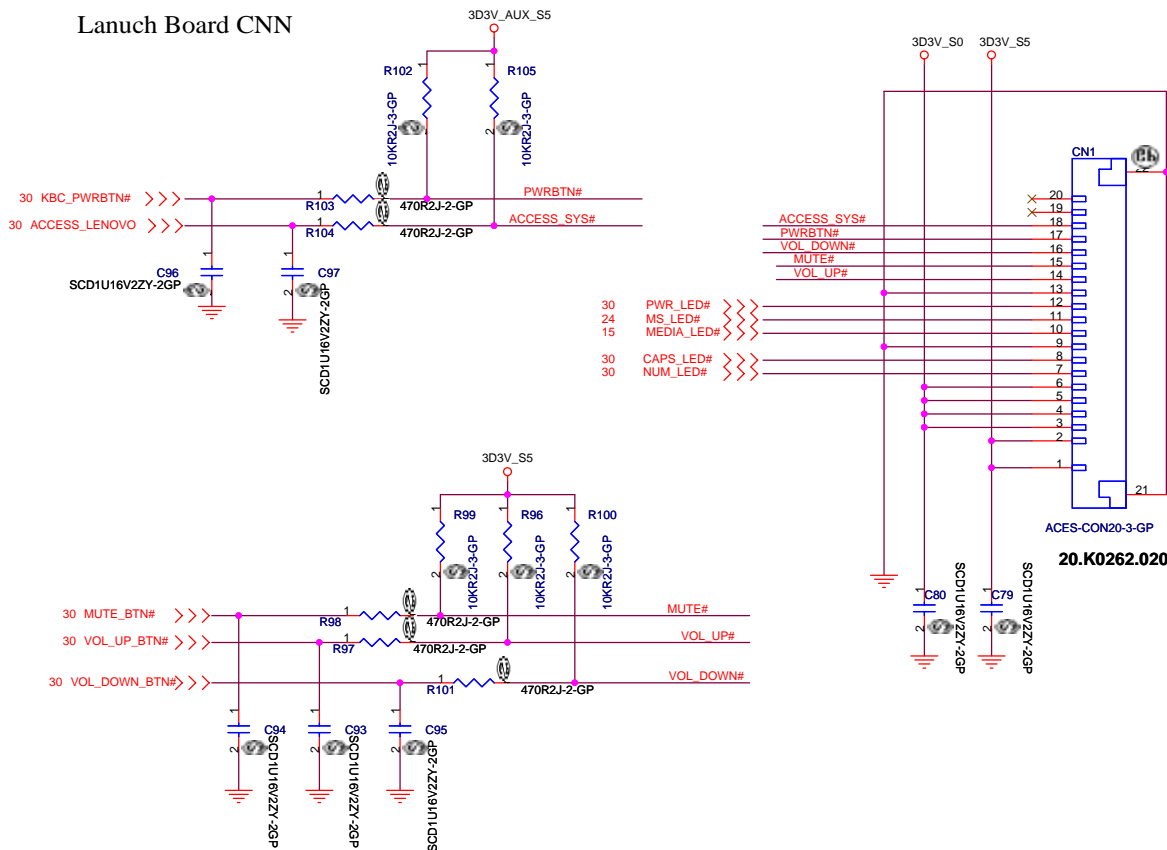
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title BIOS ROM/G-Sensor		
Size A3	Document Number A-NOTE2.0-AMD	Rev SA
Date: Tuesday, September 26, 2006	Sheet 31	of 55

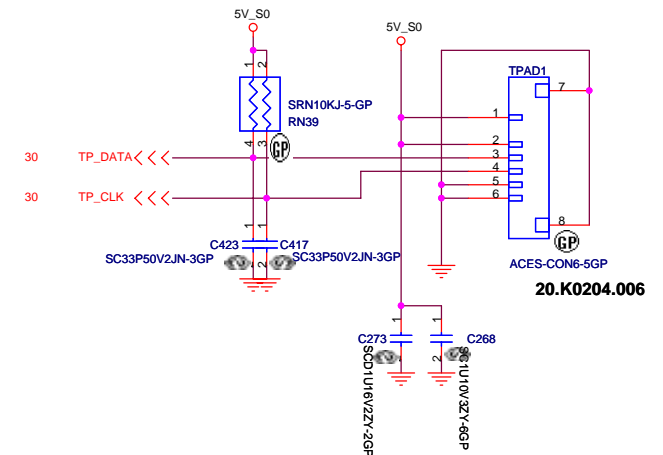
Internal KeyBoard Connector



Lanuch Board CNN



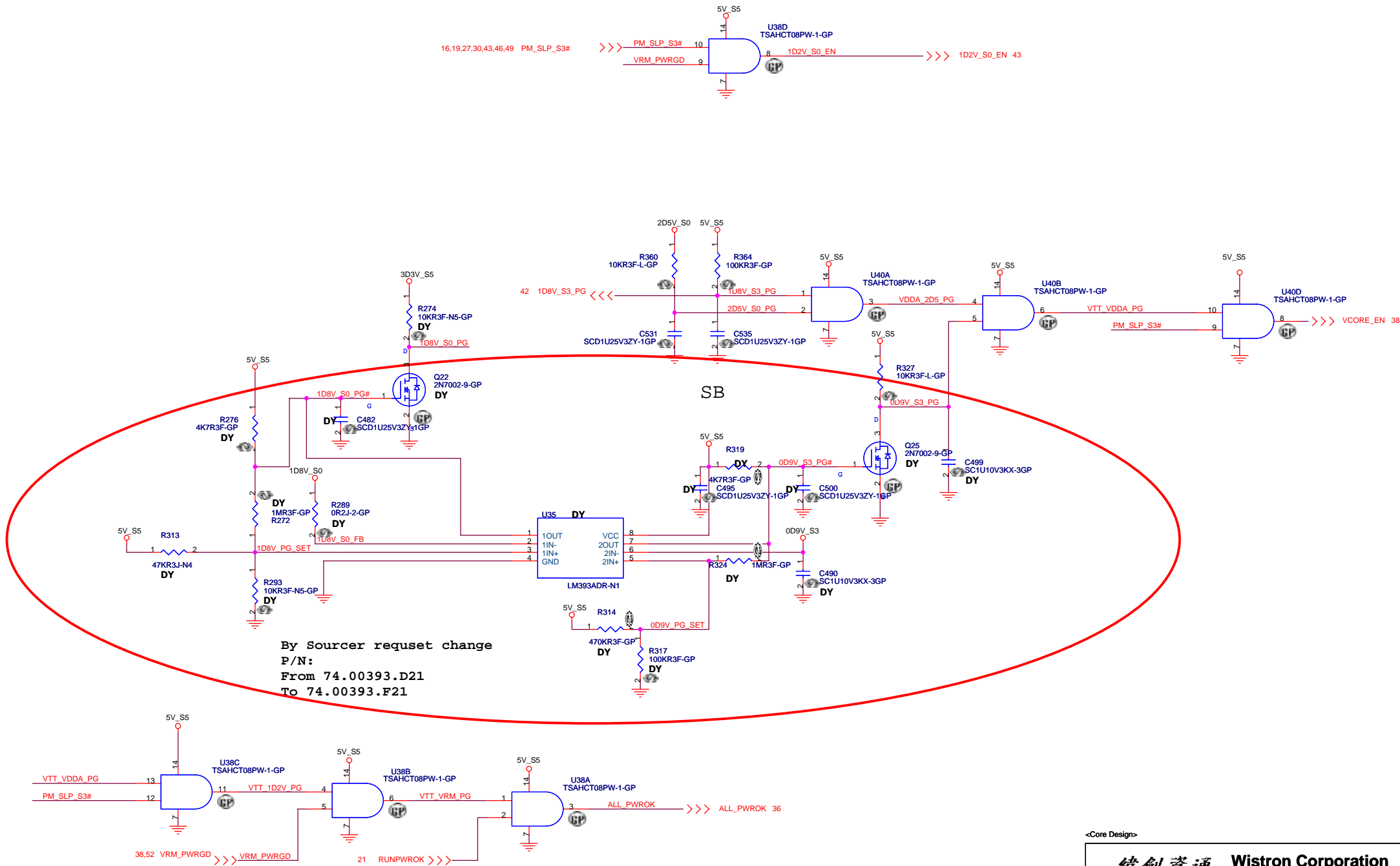
TOUCH PAD



<Core Design>

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Title LAUNCH / TOUCHPAD / KB CONN		
Size A3	Document Number A-NOTE2.0-AMD	Rev SA
Date: Tuesday, September 26, 2006	Sheet 32 of 55	



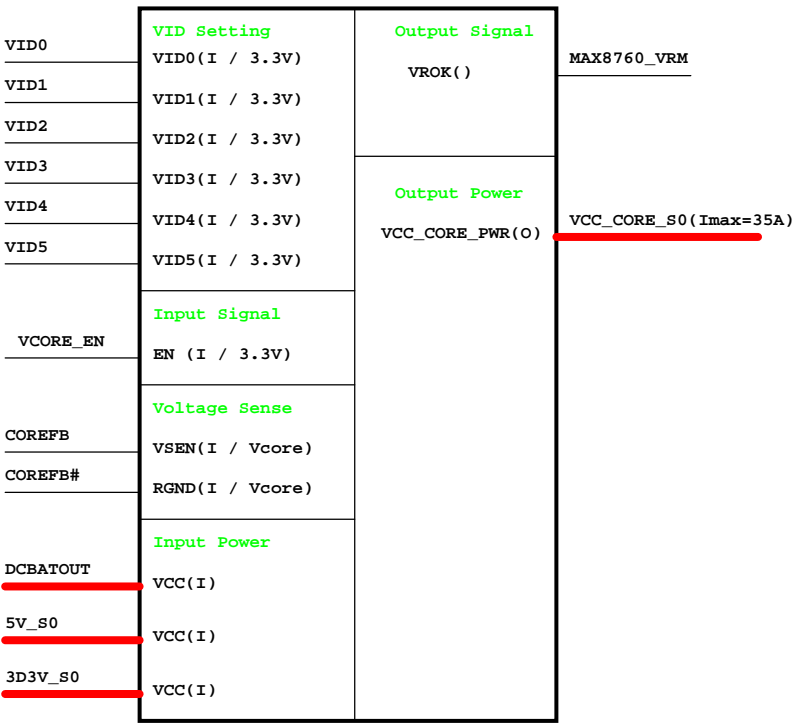
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Taipei Hsien 221, Taiwan, R.O.C.

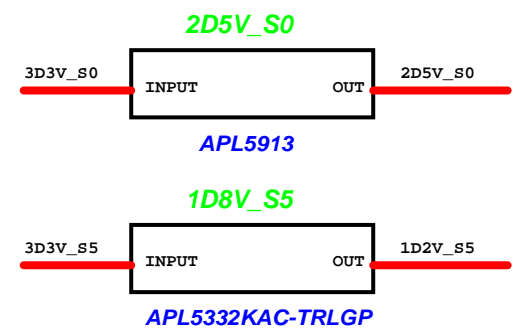
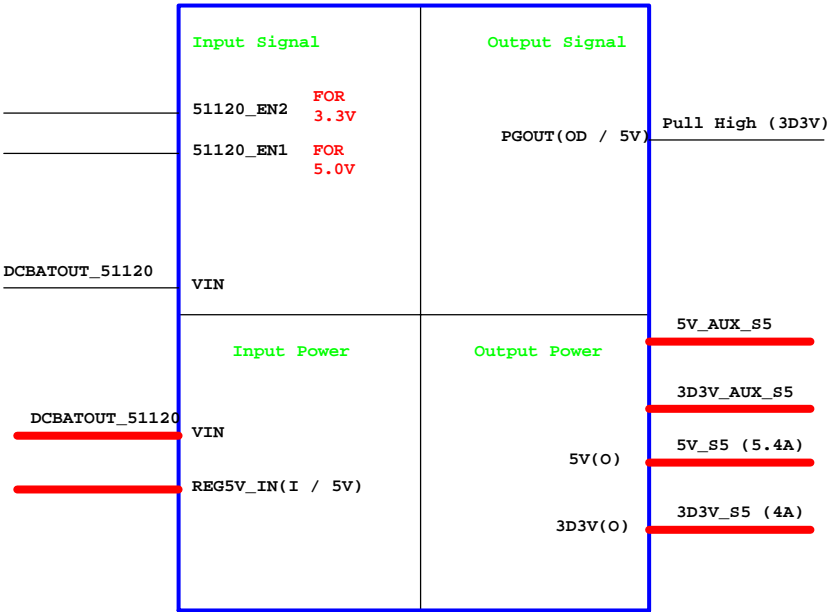
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Size	Document Number	Rev	
Custom		A-NOTE2.0-AMD	
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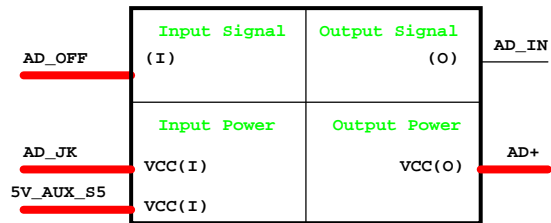
CPU_CORE
ISL6264CRZ



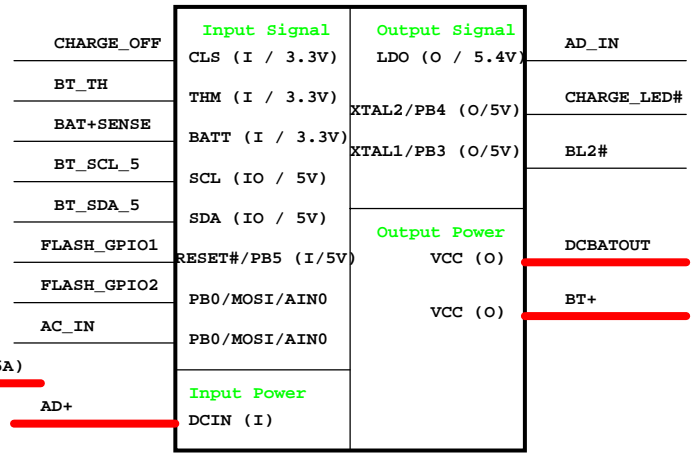
TI TPS51120
3D3V/5V



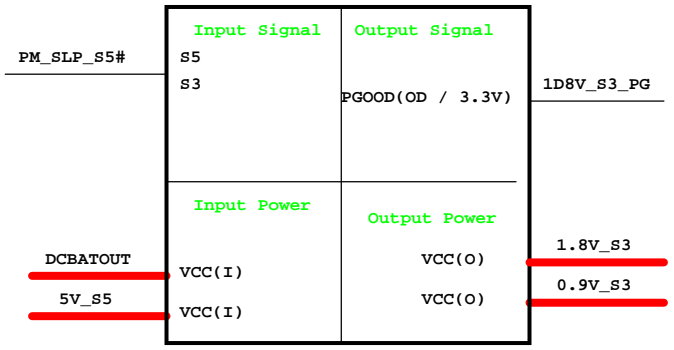
Adapter



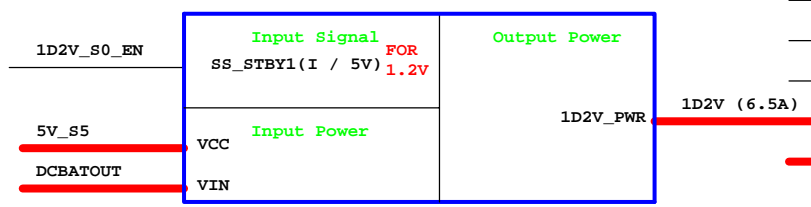
Charger_ISL6255



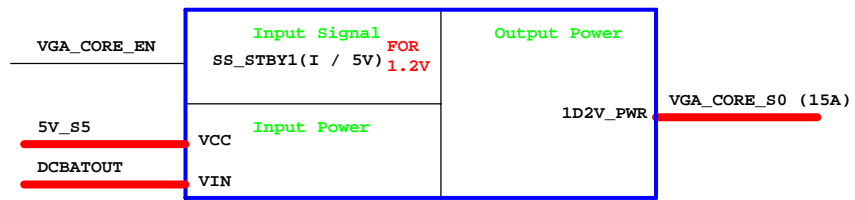
TI TPS51116
1.8V / 0.9V



ISL6268_1D2V



ISL6268_VGA_CORE



<Core Design>

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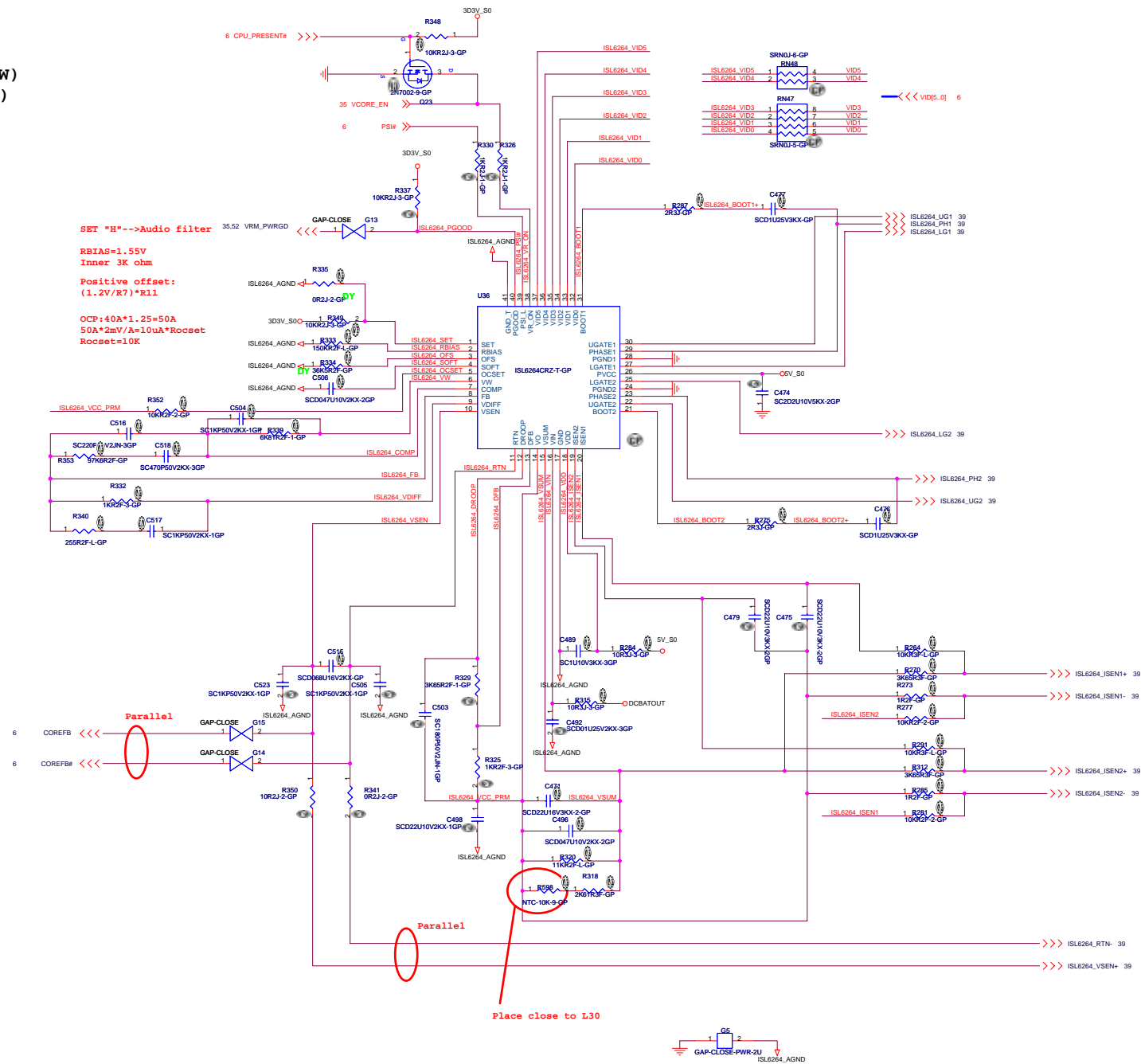
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Power Block Diagram

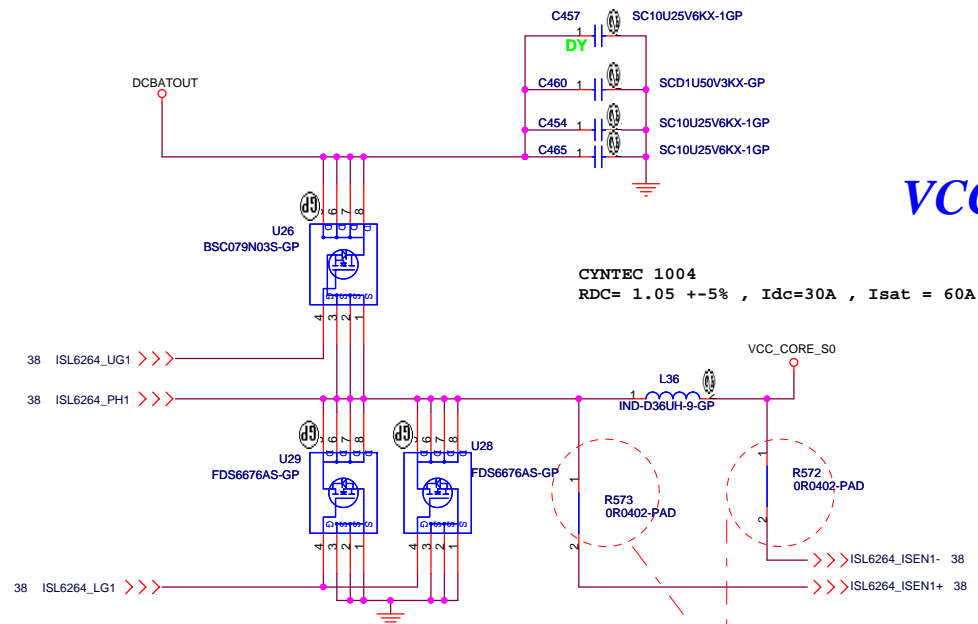
Size A3 Document Number A-NOTE2.0-AMD Rev SA

Date: Tuesday, September 26, 2006 Sheet 37 of 55

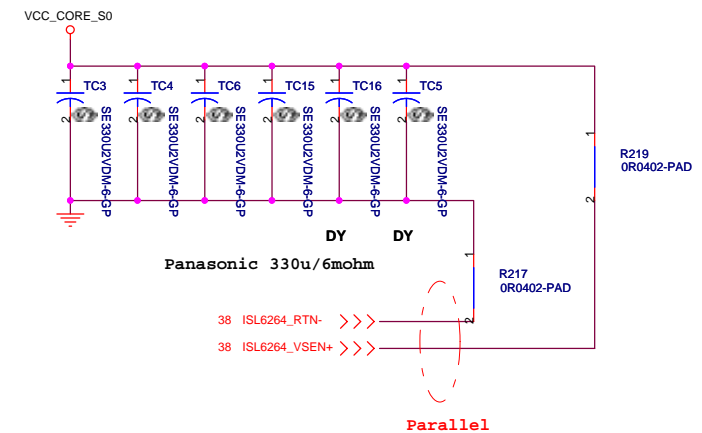
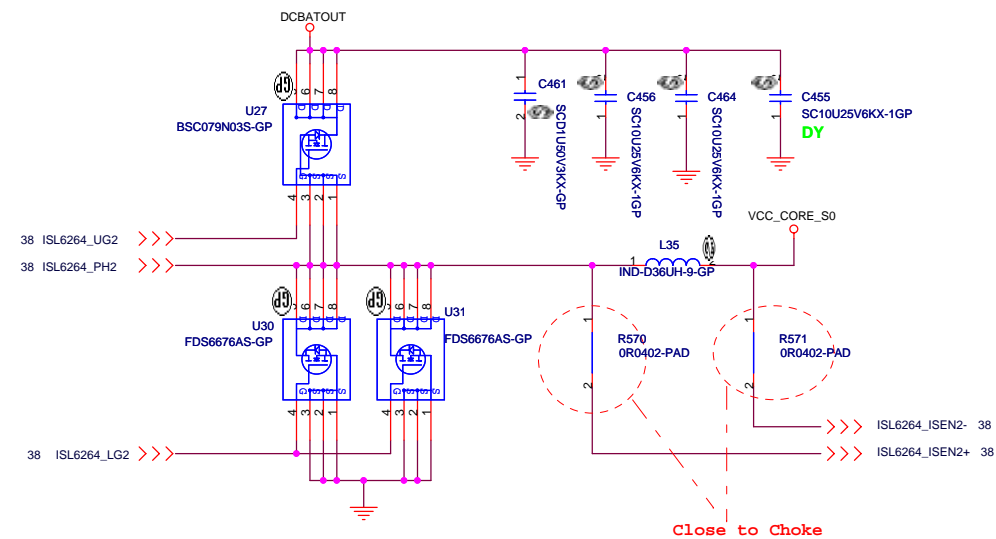
VID=1.20V(25W)/1.15V(35W)
Iomax=21A(25W)/35A (35W)
OCP=40A~45A

VID5	VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	0	1.550
0	0	0	0	0	1	1.525
0	0	0	0	1	0	1.500
0	0	0	0	1	1	1.475
0	0	0	1	0	0	1.450
0	0	0	1	0	1	1.425
0	0	0	1	1	0	1.400
0	0	1	0	0	0	1.375
0	0	1	0	0	1	1.350
0	0	1	0	1	0	1.325
0	0	1	0	1	1	1.300
0	0	1	1	0	1	1.275
0	0	1	1	0	0	1.250
0	0	1	1	1	0	1.225
0	0	1	1	1	1	1.200
0	0	1	1	1	1	1.175
0	1	0	0	0	0	1.150
0	1	0	0	0	1	1.125
0	1	0	0	1	0	1.100
0	1	0	0	1	1	1.075
0	1	0	1	0	0	1.050
0	1	0	1	0	1	1.025
0	1	0	1	1	0	1.000
0	1	0	1	1	1	0.975
0	1	1	0	0	0	0.950
0	1	1	0	0	1	0.925
0	1	1	0	1	0	0.900
0	1	1	0	1	1	0.875
0	1	1	1	0	0	0.850
0	1	1	1	0	1	0.825
0	1	1	1	1	0	0.800
0	1	1	1	1	1	0.775
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.75
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.725
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7
1	1	1	1	1	1	0.375





VCC_CORE_S0



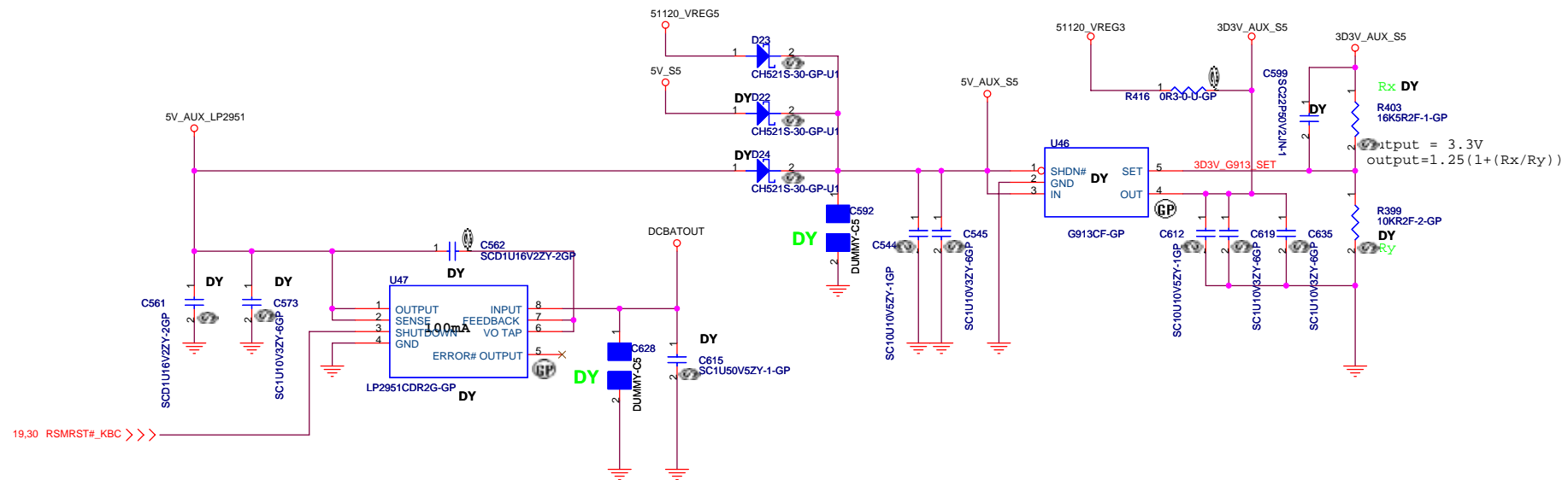
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Title			
CPU Vcore Power_2			
Size	Document Number		Rev
A3	A-NOTE2.0-AMD		SA
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Aux Power

3D3V_AUX_S5

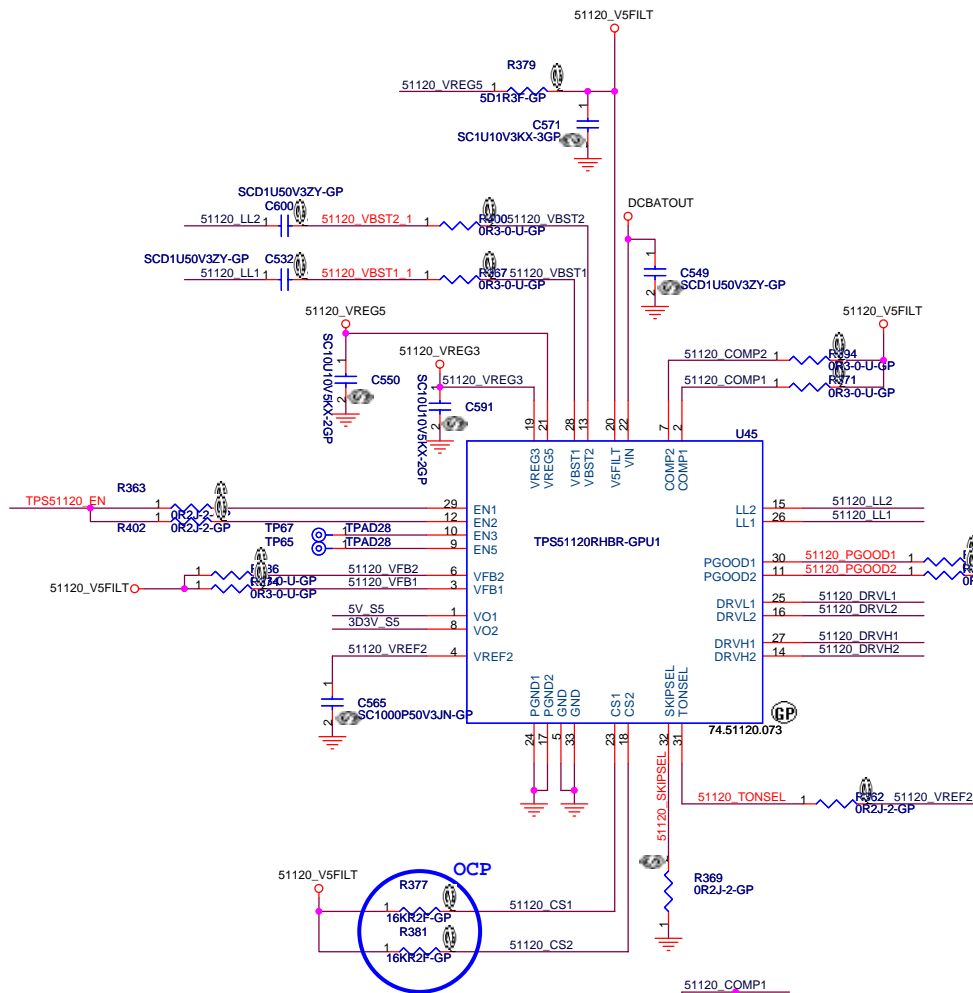


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Title		
3D3V/ 5V AUX		
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$I_d = 9.2A$
 $Q_g = 9 \sim 12nC$,
 $R_{ds(on)} = 17.4 \sim 22m\Omega$

$I_d = 9.6A$
 $Q_g = 18 \sim nC$,
 $R_{ds(on)} = 13.5 \sim 16.5m\Omega$

$I_d = 9.2A$
 $Q_g = 9 \sim 12nC$,
 $R_{ds(on)} = 17.4 \sim 22m\Omega$

$I_d = 9.6A$
 $Q_g = 18 \sim nC$,
 $R_{ds(on)} = 13.5 \sim 16.5m\Omega$

**5V $I_{omax} = 6A$
 $OCP > 10A$**

**3D3V $I_{omax} = 6A$
 $OCP > 10A$**

$$V_{out} = 1V * (R1 + R2) / R2$$

For TPS51120,
 $V_{out} = 5V$
 1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
 2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
 3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
 $V_{out} = 3.3V$
 1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
 2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
 3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

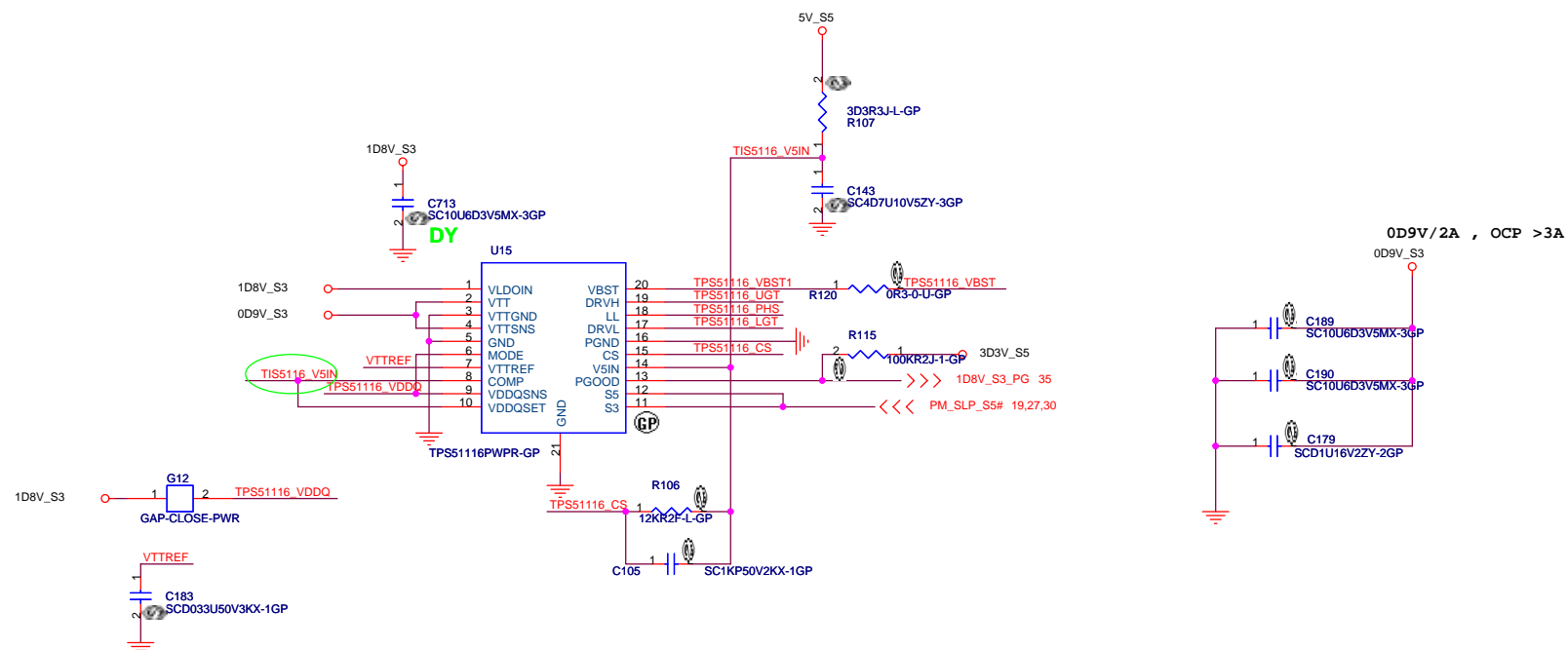
Pin	GND	VREF2	FLOAT	V5FILT
COMP	N/A	N/A	Current Mode (apply R-C network)	D-CAP. Mode
TONSEL (CH1/CH2) [kHz]	380 / 580	280 / 430	220 / 330	180 / 270
VFB1	Adjustable output (connect to the resistor divider)			5V fixed output
VFB2	Adjustable output (connect to the resistor divider)			3.3V fixed output
SKIPSEL	AUTO-SKIP	AUTO-SKIP (FAULTS OFF)	PWM	PWM
EN1, EN2	Switcher Off	Not used	Switcher on	Switcher on

<Core Design>

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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **TI TPS51120 3D3V/5V**
 Size A3 Document Number: **A-NOTE2.0-AMD** Rev **SA**
 Date: Tuesday, September 26, 2006 Sheet 41 of 55

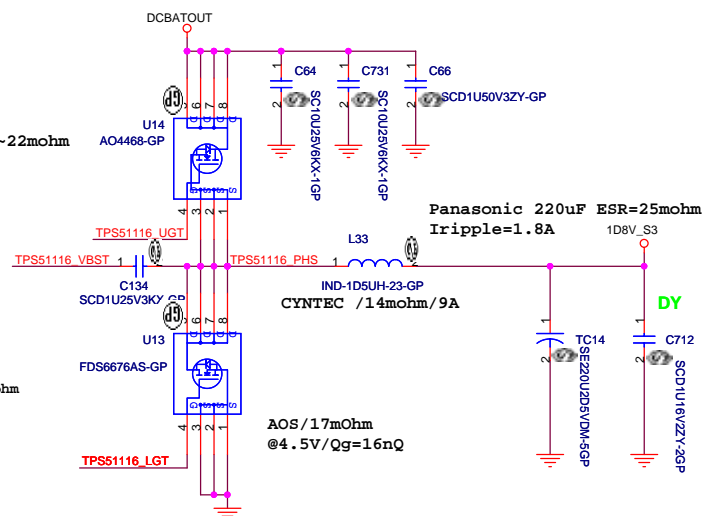
TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm

Id=13A
Qg=18 ~ 27nC,
Rdson=7.5 ~ 8.7mohm



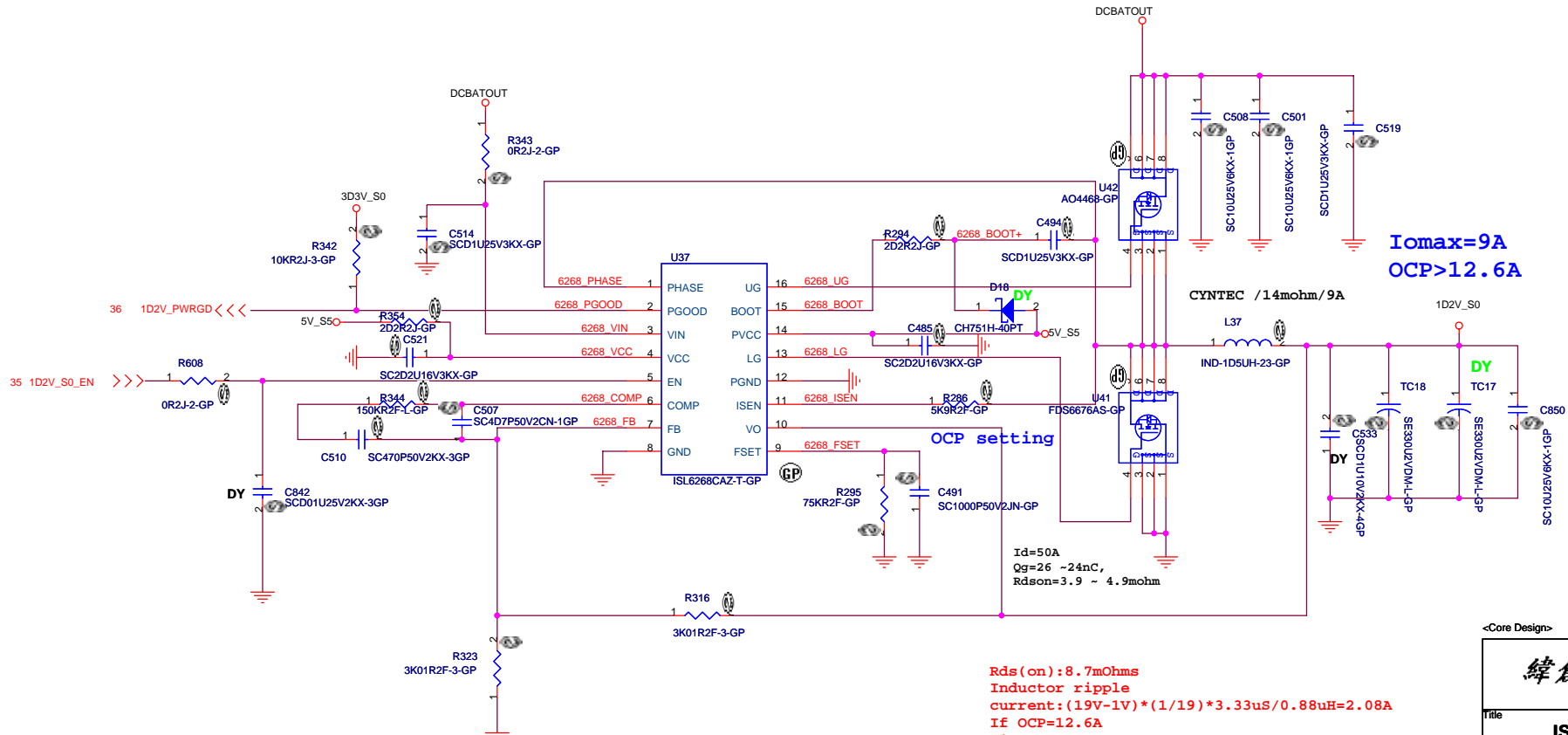
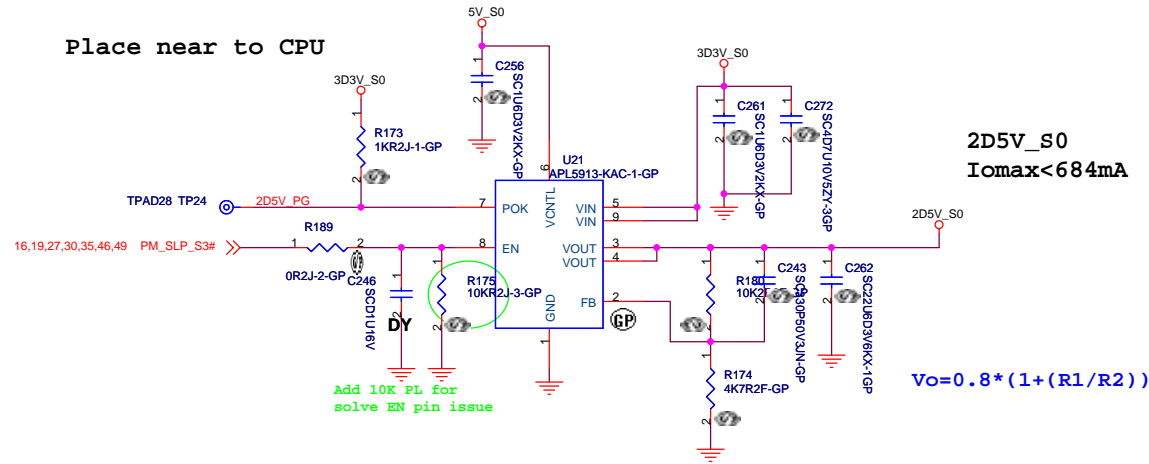
1D8V/9A , OCP >15A

<Core Design>

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Title			
TI TPS51116 1D8V / 0D9V			
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Place near to CPU

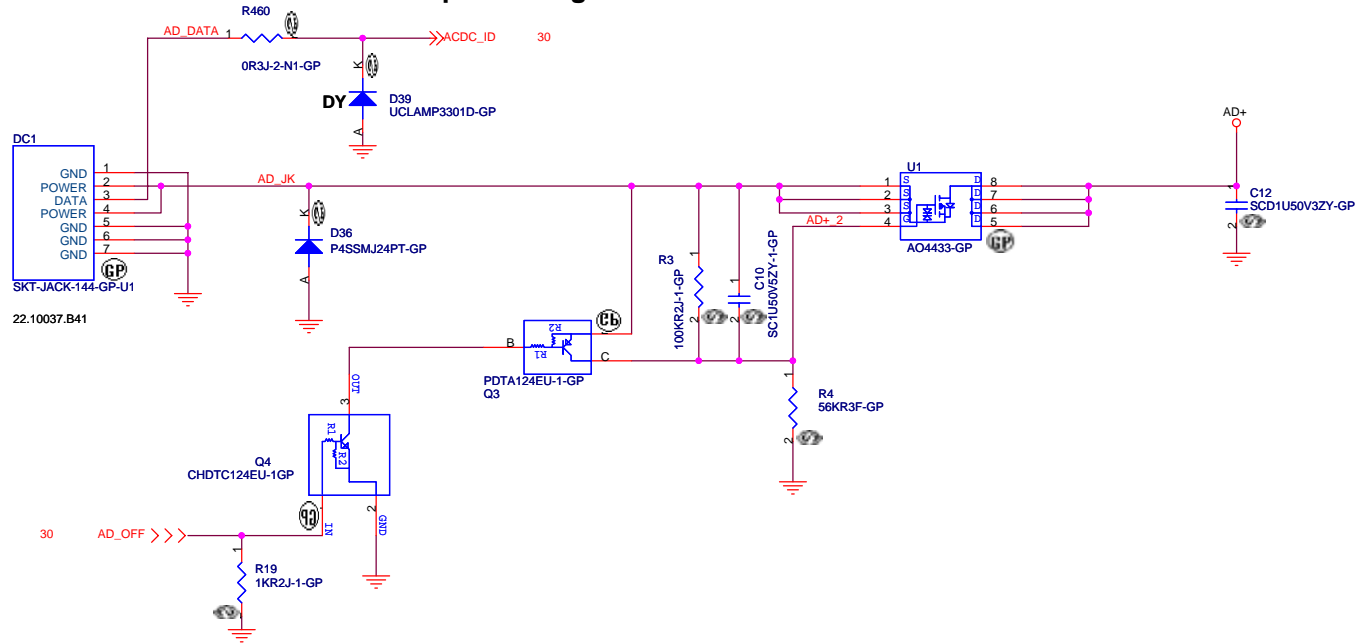


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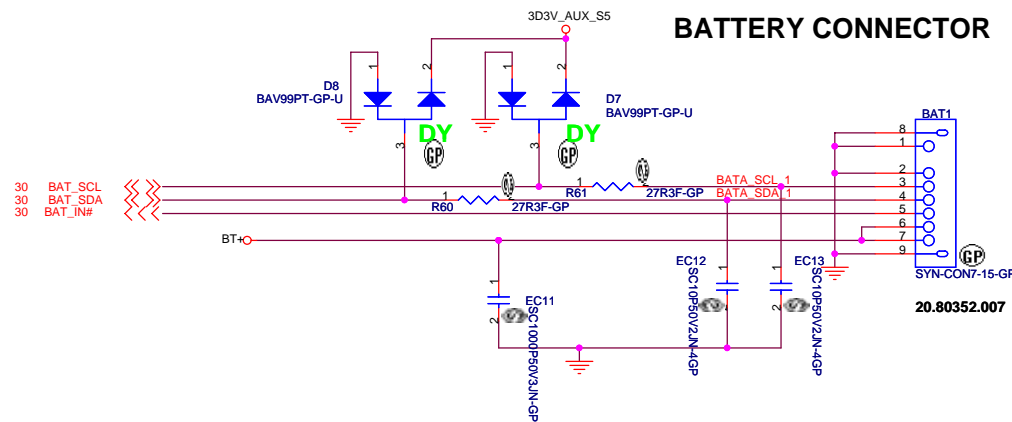
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
ISL6268 1D2V		
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Adaptor in to generate DCBATOUT



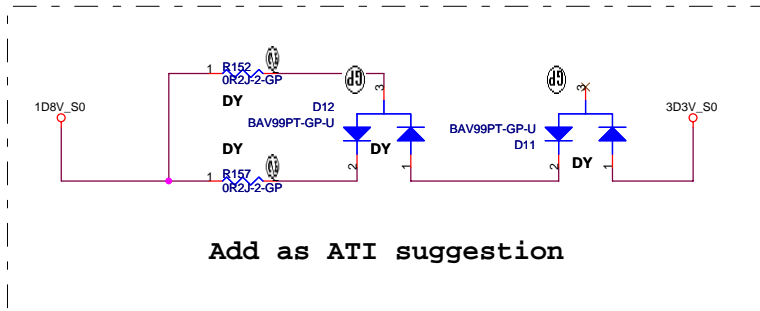
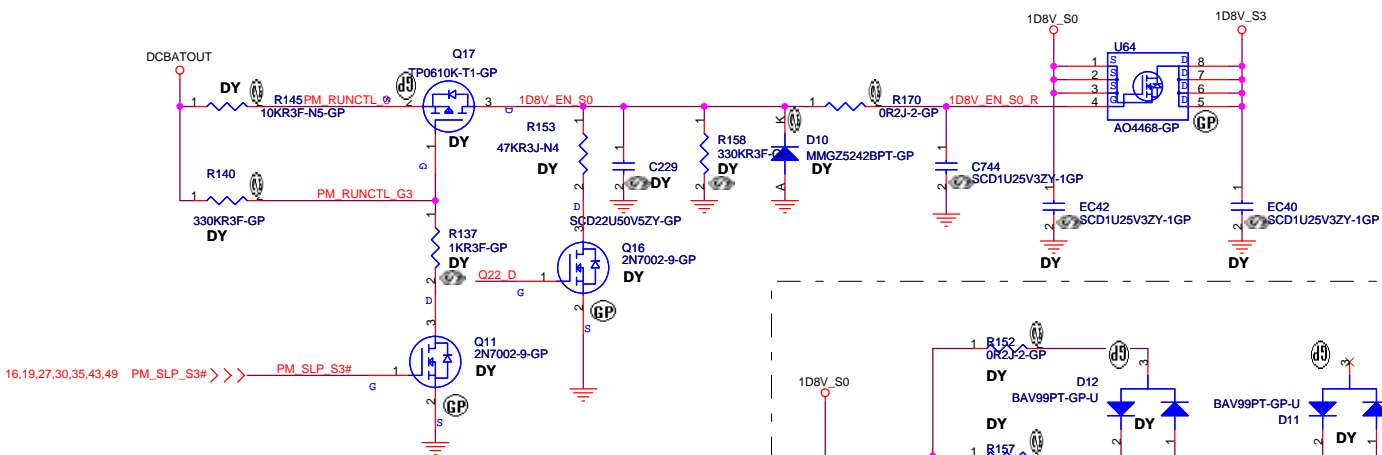
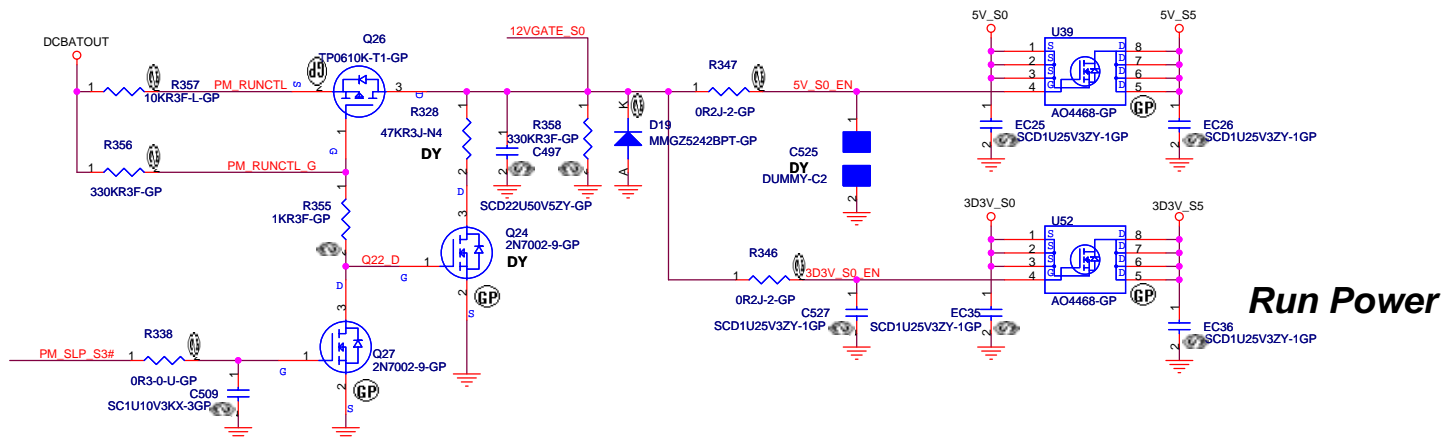
BATTERY CONNECTOR

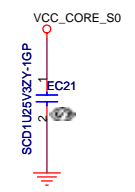
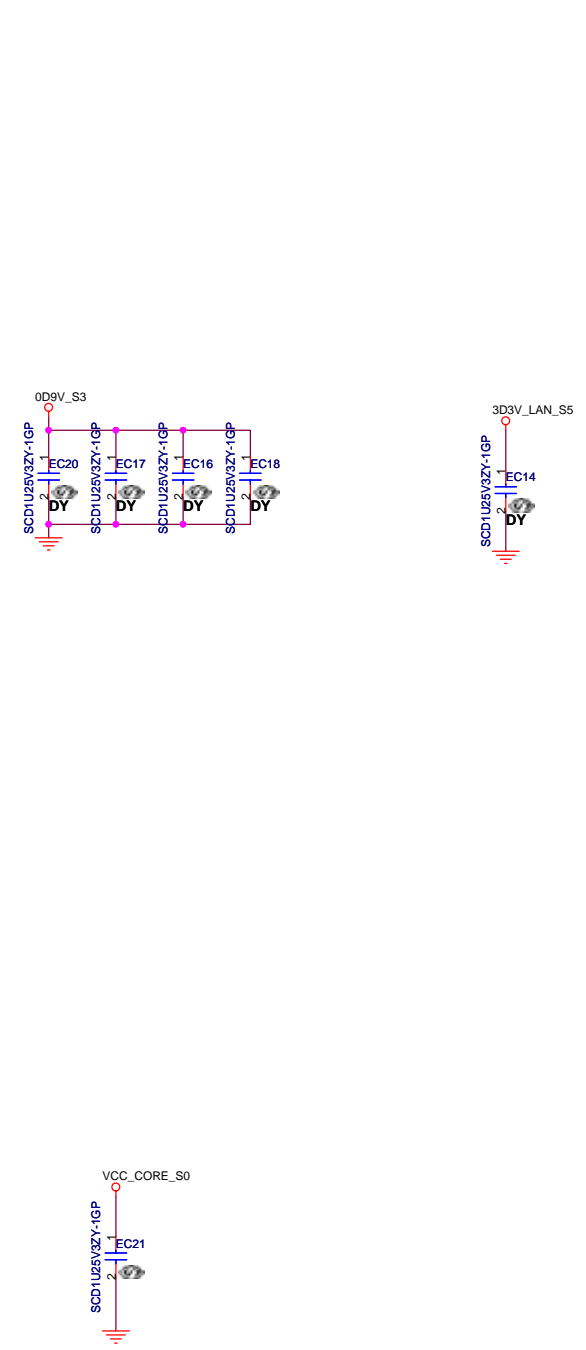
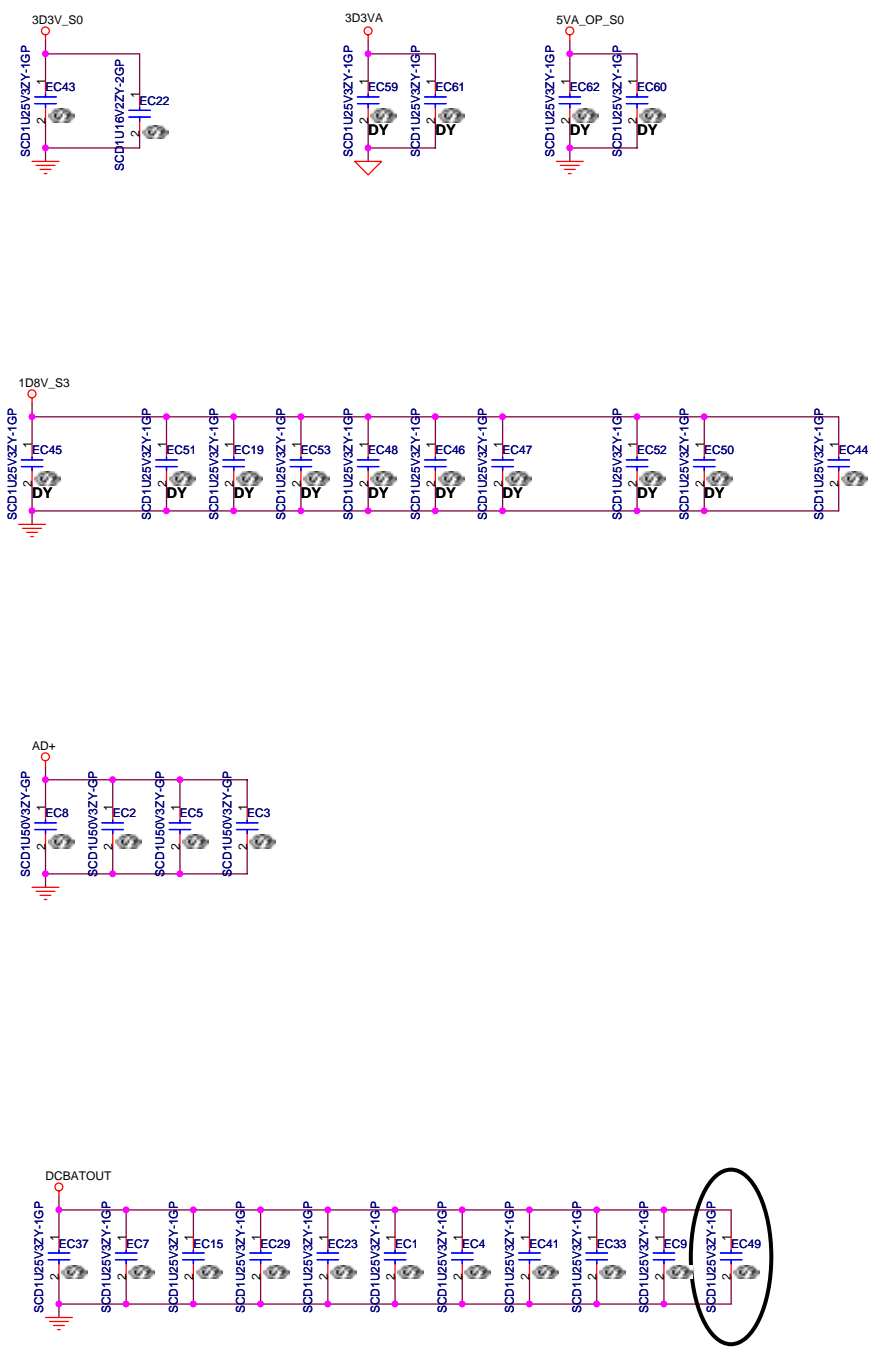


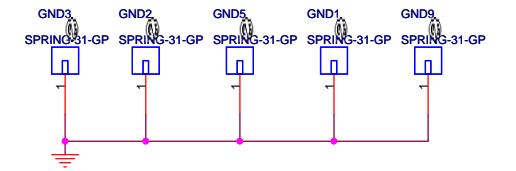
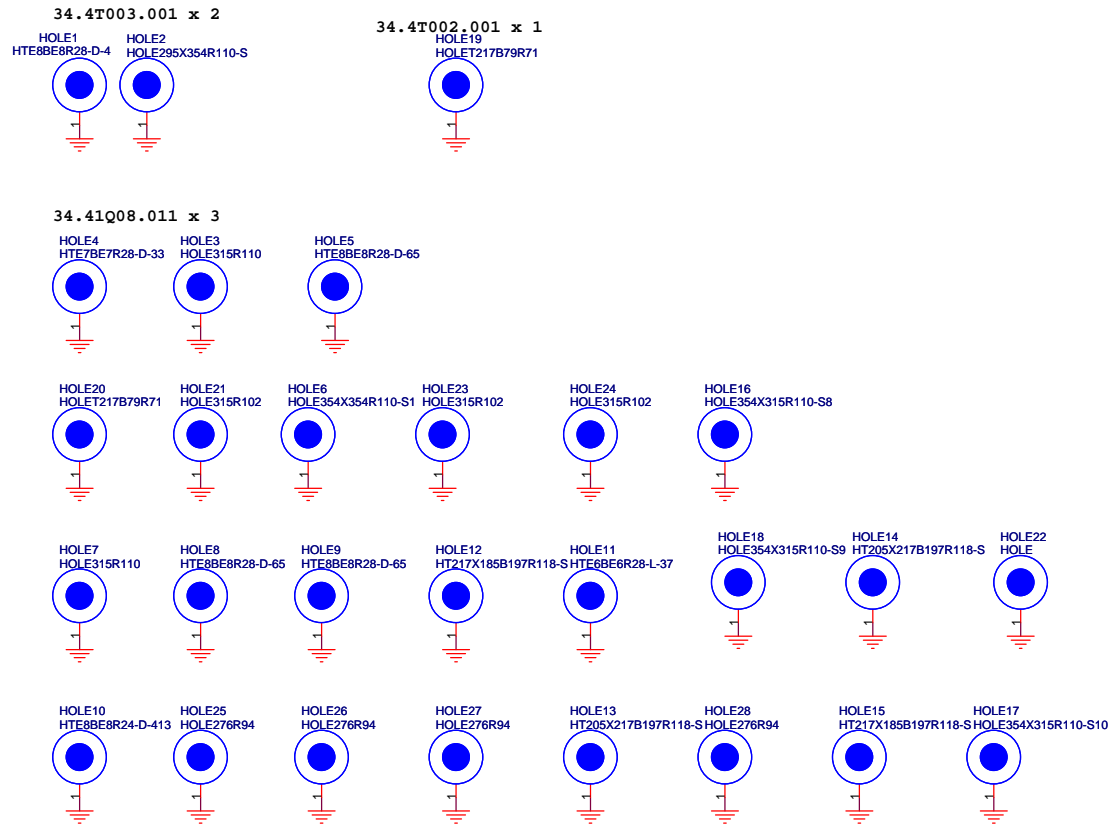
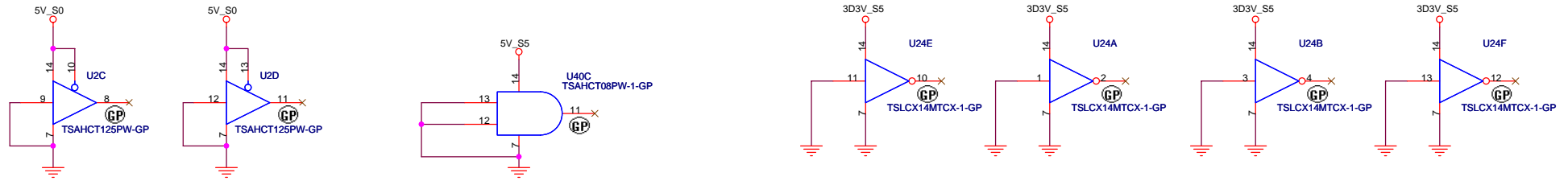
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Taipei Hsien 221, Taiwan, R.O.C.

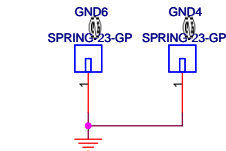
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AD/BAT CONN			
Size	Document Number		Rev
A3	A-NOTE2.0-AMD		SA
Date: Tuesday, September 26, 2006		Sheet 45 of 55	



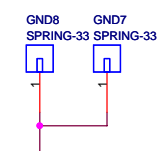




34.49U24.001 x 5



34.39S07.001 x 2



34.4B312.001 x 2

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

MISC

Size
A3

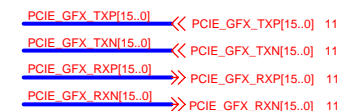
Document Number

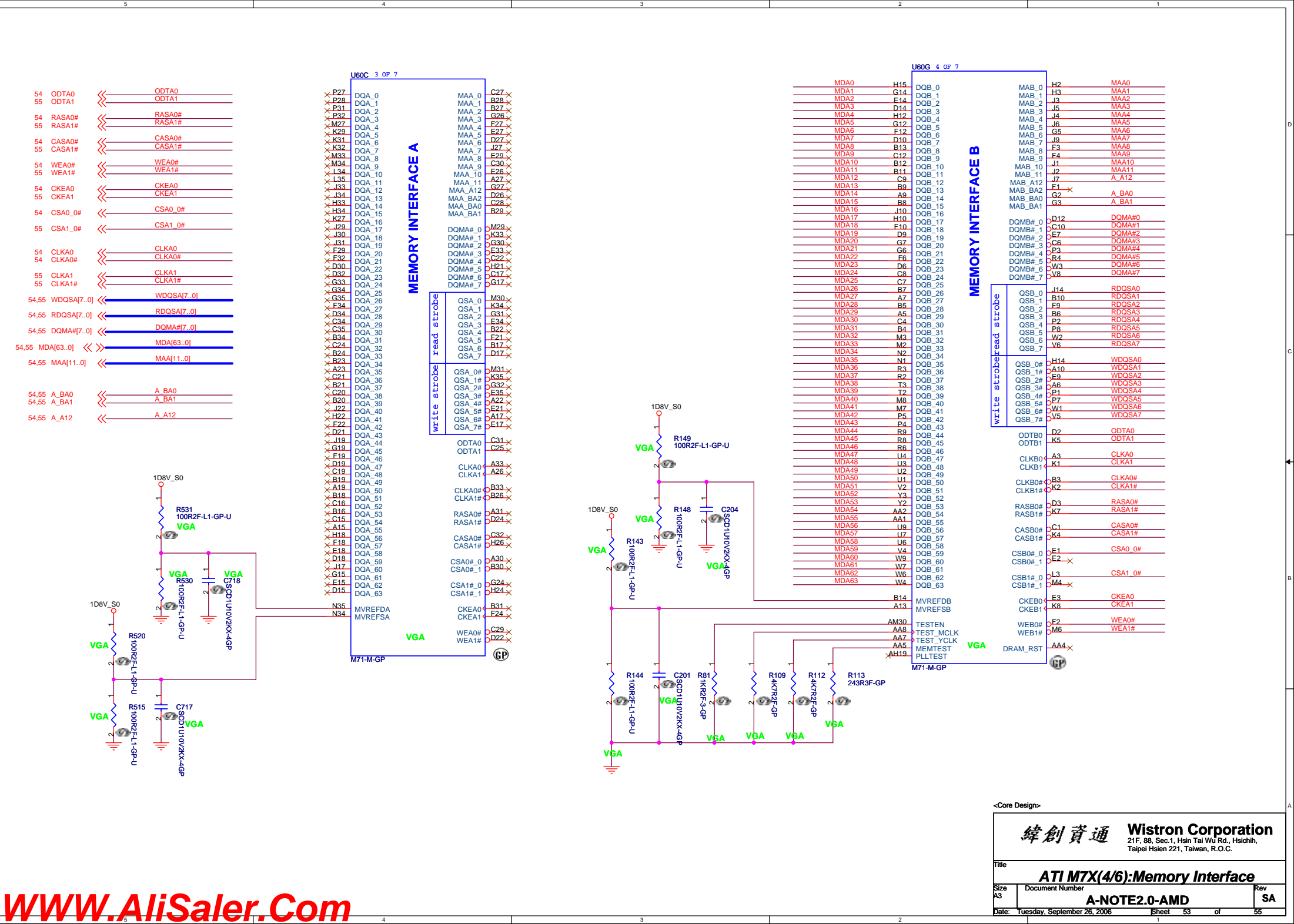
A-NOTE2.0-AMD

Rev
SA

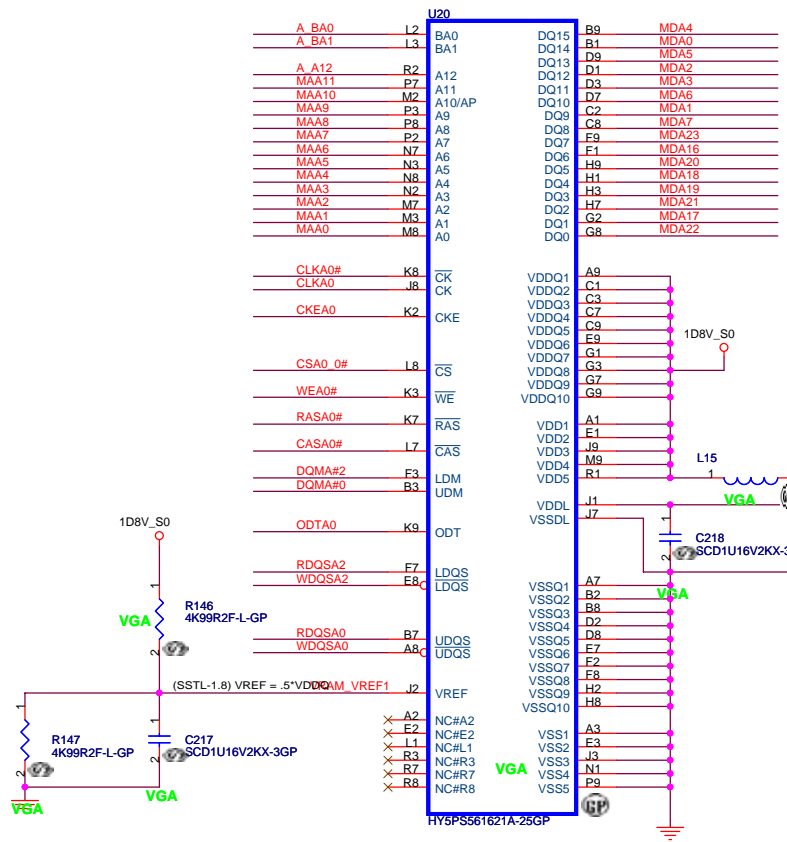
Date: Tuesday, September 26, 2006

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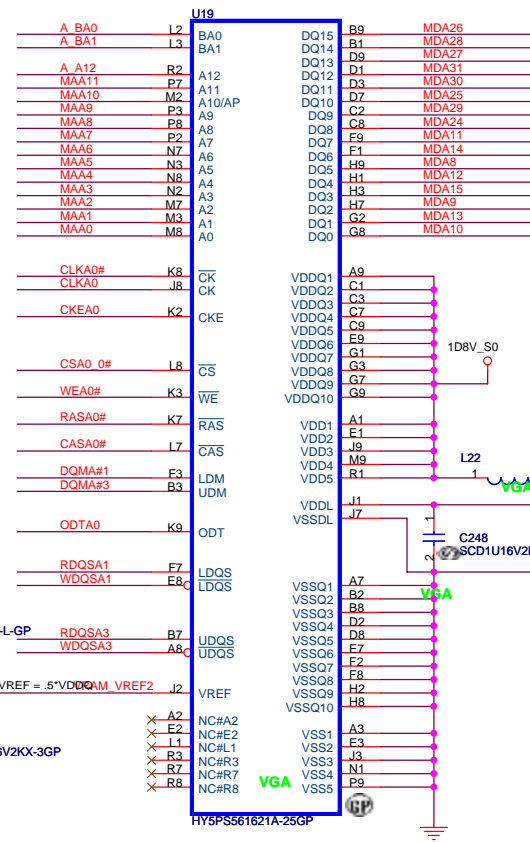




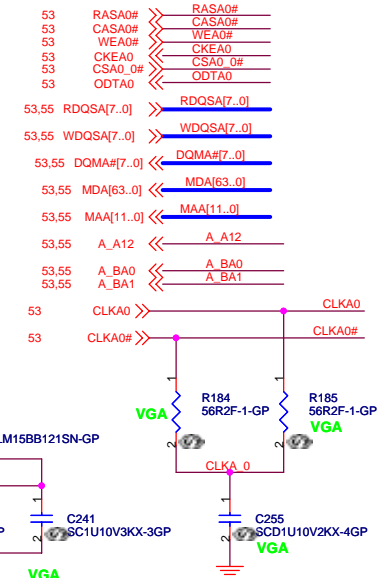
DDR2 BGA MEMORY



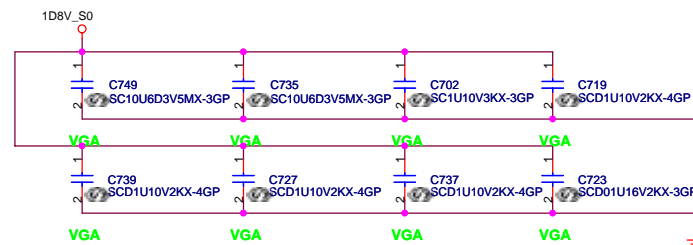
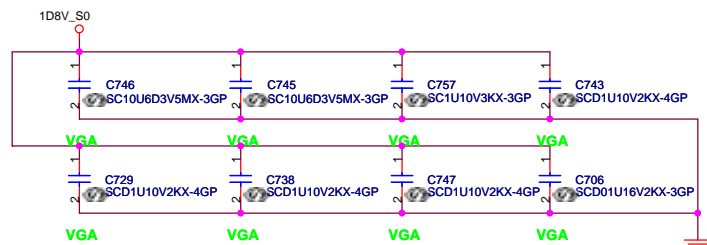
72.55616.C0U



72.55616.C0U



Hynix	256Mb-->LAB1 use	72.55616.C0U
	512Mb	72.51216.D0U
Second Source	256Mb-->LAB1 use	72.18256.B0U
Qimonda	512Mb	72.18512.A0U

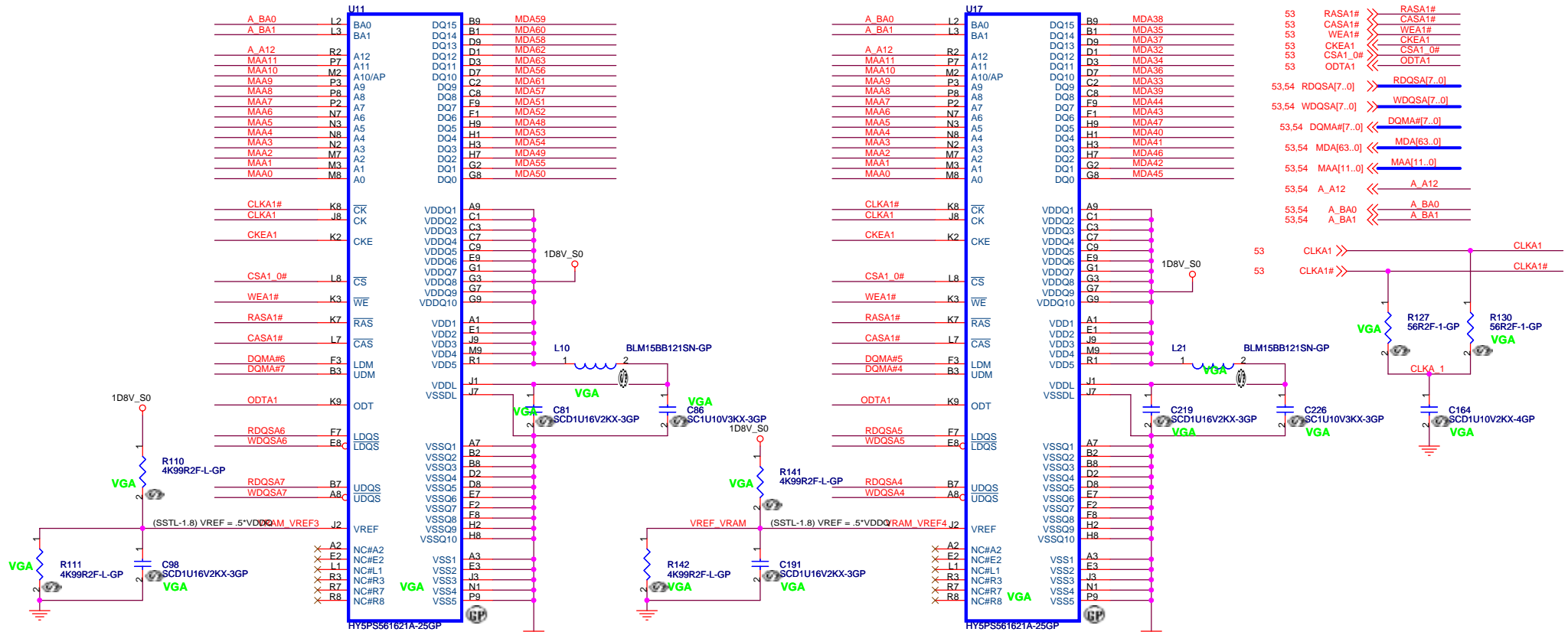


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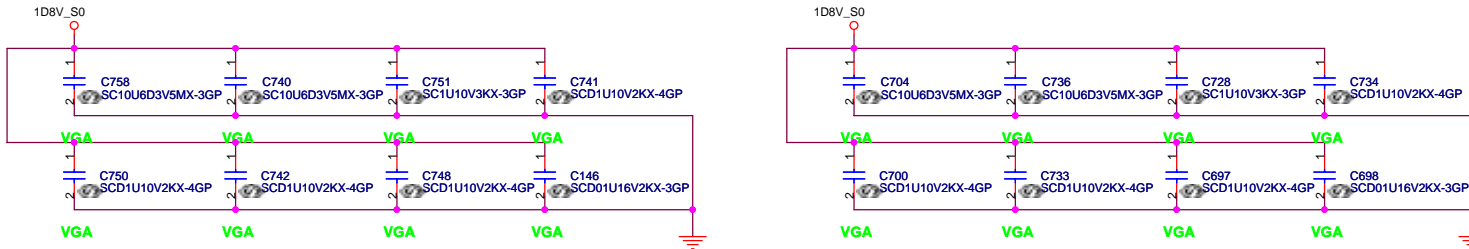
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DDR2 BGA MEMORY



72.55616.C0U

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